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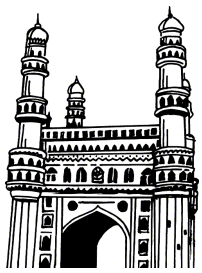

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**Logic gates:** OR, AND, NOT gates, truth tables, realization of these gates using discrete components. NAND, NOR as universal gates, Exclusive – OR gate (EX-OR). DeMorgan's Laws – Verification.

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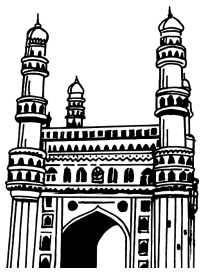

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**Diodes:**
P-N junction diode, Half-wave, full-wave and bridge rectifier. Zener diode & its characteristics. Zener diode as voltage regulator.

## 1.1 Introduction of Band Theory

**Q1. Explain the Introduction of Energy band?**

*Ans :*

In case of solids, the atoms are arranged in a systematic space lattice and hence the atom is greatly influenced by neighbouring atoms. The closeness of atoms results in the intermining of electrons of neighbouring atoms, of course, for the valence electrons in the outermost shells which are not strongly bounded by nucleus.

Due to intermining the number of permissible energy levels increases. Hence in case of a solids, instead of single energy levels associated with the single atom, there will be bands of energy levels. A set of such closely packed energy levels is called an energy band.

## 1.2 Energy Band in Solids, Valence Band, Conduction Band & Forbidden Energy gap in Solids

**Q2. Explain valence Band, Conduction Band & forbidden Energy gap ?**

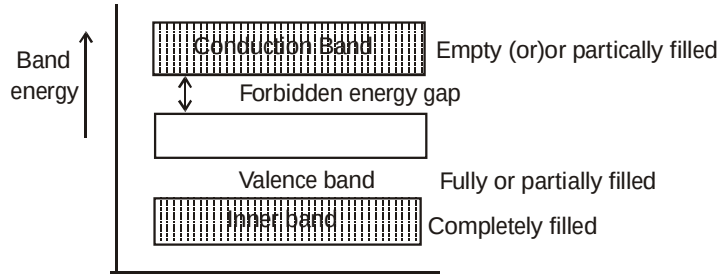
*Ans :*

**(i) Valence Band**

We know that the atoms of a solid are arranged in a regular repeated geometric pattern and the electrons of the atoms rotated around their nuclei in certain permitted energy levels. The electrons in the shell are strongly to their nuclei. The electrons in the outermost shell are called valence electrons. The band formed bounded a series of energy levels containing the valence electrons is known as Valence band.

The valence band may be defined as a band which is occupied by the valence electrons or a band having highest occupied band energy.

The valence band is shown in fig. The valence band may be partially or completely filled upon the nature of the crystal. This band can never be empty.



**(ii) Conduction Band**

In certain materials (metals), the valence electrons are loosely attached to the nucleus. Even at ordinary temperature, some of valence electrons leave the valence band. These are called free electrons. These are responsible for the conduction of current in a conductor and hence also called as conduction electrons. The band occupied by these electrons is called conduction band as shown in fig. The band is next to the valence band.

The conduction band may also be defined as the lowest unfilled energy band. This band may be empty or partially filled. In conduction band, the electrons can move freely, when a substance has empty conduction band, the current conduction is not possible. Generally, insulators have empty conduction band.

**(iii) Forbidden Energy Gap**

The separation between conduction band and valence band is known as forbidden energy gap. There is no allowed energy state in this gap and hence no electron can stay is the forbidden energy gap.

It should be remembered that greater is the energy gap, more tightly the valence electrons are bounded to the nucleus. In order to push an electrons from valence band to conduction band, external is required which is equal to the forbidden energy gap.

## 1.2.1 Insulators, conductors & Semi- conductors

**Q3. Discuss on the basis of forbidden band about insulators, conductors & semi- conductors?**

*Ans :* **(Imp.)**

On the basis of forbidden band, the insulator, semi conductors and conductors are described as follows :

- **Insulators**

The substance which don't allow the passage of current through them are called insulator. For example, glass, wood plastic, rubber, mica, ceramic etc., are insulator. In case of insulator, forbidden energy band is very wide. Due to this fact electron cannot jump from valence band to conduction band.

In insulator the valence electron are bounded very tightly to their parent atom. For example, in case of materials like glass, the valence band is completely full at $0^{o}$ K and the energy gap between valence band and conduction band is of the order of 10 ev.

Even in the presence of high electric field the electron don't move from valence band to conduction band. When a very high energy is supplied, an electron may be able to jump across the forbidden gap. Increase in temperature enable some electron to got to conduction band. This explain why certain material which are insulator to room temperature become conductor at high temperature. The resistivity of insulator of the order of $10^{-7}$ ohm meter.

- **Conductors**

In case of conductor there is no forbidden band and the valence band and conduction band overlap each other. Here plenty of free electron are available for electric conduction. The electron from valence band freely enter in the conduction band.

Due to the overlapping of valence and conduction band, a different across the conduction cause the free electron to constitute electric current. The most important point in conductors is that due to the absence of forbidden band there is no structure to establish holes. The total current in conductors is simply a flow of electrons.

- **Semi Conductors**

In semiconductor the forbidden band is very small Germanium and silicon are the example of semi conduction. In germanium the forbidden band is of the order of 0.72 ev while in case of silicon the forbidden band is of the order of 1.12 ev.

Actually a semiconductor material is one whose electricity or properties lies b/w insulator and good conductors. At $0^{o}$.K there are no electrons in conduction band the valence band is completely filled.

When a small amount of energy is supplied the electron can easily jump from valence band to conduction band. For example, when the temperature is increased the forbidden band is decreased, so that same electron are liberated into the conduction band.

In semi conductor, the conductivity are of the order of $10^{2}$ mho. metre.

**Q4. Distinguish between conductors, Insulators, Semi conductor based on different parameters?**

*Ans :*

Comparison of conductors, Insulators & Semi conductors.

| S.No. | Parameter | Conductors | Insulators | Semi Conductors |
|---|---|---|---|---|
| 1. | Conductivity | Very high | Very low | Moderate |
| 2. | Resistivity | Very low | Very high | Moderate |
| 3. | Forbidden gap | No forbidden gap | Large gap | Moderate |
| 4. | No. of electrons available for conduction. | Very large | Very small | Moderate |
| 5. | Conductivity at room temperature | Very good | Poor | Moderate |
| 6. | Temperature Co-efficient of resistance | Positive | Negative | Negative |
| 7. | Examples | Copper, Aluminium etc. | Glass, paper mica, etc. | Silicon, Germanium etc. |
| 8. | Application | Conductor, wires etc. | Capacitors, Insulation for wire etc. | Semi- conductors devices etc. |



## 1.3 Intrinsic & Extrinsic Semiconductors

**Q5. Explain Instrinsic & Extrinsic Semiconductors?**

*Ans :*

Semi conductors are broadly classified into two types namely.

i) Extrinsic semi conductors

ii) Extrinsic semi conductors

### (i) Intrinsic semiconductors

This type of semiconductor is made out of the semiconductor material in its extreme pure form.

**Ex :** Ge and Si which have forbidden energy gaps of 0.72 ev and 1.1 ev respectively.

When an electric field is applied to an intrinsic semiconductor at a temperature greater than $0^o$ K, the electrons in conduction band move towards the anode and also the holes in the valence band move towards the cathode.

An intrinsic semiconductor may be defined as a material in which the number of conduction electrons are equal to the number of holes.

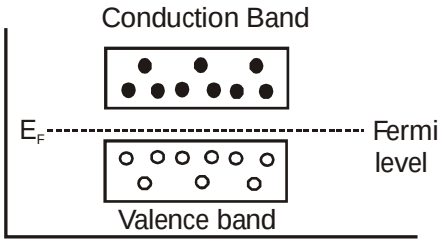



**Fig :. Energy Band Diagram of an Intrinsic Semiconductor at Room Temperature**

### (ii) Extrinsic Semi Conductors

The inpure form of Semiconductor formed by adding external impurities tot he intrinsic semiconductor is known as extrinsic semiconductor. In other words, it is an intrinsic semiconductor with added impurities.

In its pure form intrinsic semiconductor has very conduction current. In order to increase the conductivity of intrinsic semi conductors, certain amount of suitable impurities are added to it. Such addition of impurities to a semiconductor is known as dopping.

Depending on the type of doping material used (or) impurity added, extrinsic semiconductors are classified as,

(a) P - type semiconductors

(b) N - type semiconductors

P-type semiconductors are formed by adding trivalent impurity to a pure Germanium crystal. On the other hand, N-type semiconductors are formed by adding pentavalent impurity to a pure germanium (Ge) crystal.

## 1.4 N - Type & P - Type Semiconductor

**Q6. Explain N-type & P-type Semi conductors?**

*Ans :* **(Imp.)**

**N- type Semi conductor**

If a small amount of pentavalent impurity is added to intrinsic semi conductor crystal during the crystal growth, then the resulting crystal is known as N-type semiconductor.

The electrons are the majority carrier and holes are minority carriers in an N-type semiconductor. They are also called as donor type semiconductor because they are capable of donating an electron.

The concentration of impurity atoms added to the pure semi conductor is very small, such that one pentavalent impurity atom is surrounded by 4 atoms of Ge (or) Si (Pure semiconductor). The 5 valence electrons of impure atoms are shared by 4 Ge (or) Si to form covalent bonds. The extra 5$^{th}$ electron of the impure atom can be dislodged by supplying small range of energies (0.01 ev to 0.05 ev)

Hence, free electrons exists for every impurity atom. Thus, the number of electrons are high in this type of semiconductor.

Fig (1) shows the crystal lattice with one Ge atom displaced by As atom.

Fig (b) represents the energy band description of N-type semiconductor.

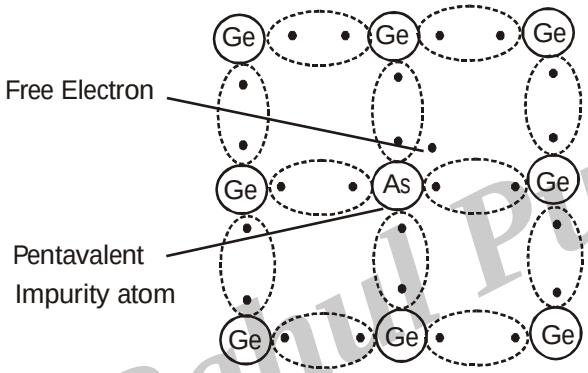
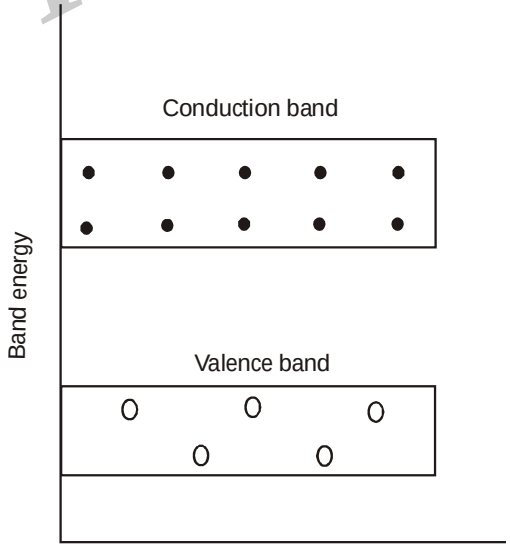



**Fig. (b) : N - type semi - conductor**




It can be observed from fig (2) that with the addition of as impurity the number of electrons in conduction band is increased greatly. Hence, the electron concentration is increased in conduction band. It exceeds the hole concentration in the valence band.

As N- type semiconductor is electrically neutral though it passes large number of electrons. Because electrons are created by adding neutral pentavalent impurity to intrinsic semiconductor (i.e. no. of positive or negative charges are added to the crystal).

### P- type Semiconductor

If a small amount of trivalent impurity is added to intrinsic semiconductor crystal during the crystal growth, then the resulting crystal is known as P-type semiconductor.

In this type of semiconductor, large number of holes are present and thus this type is always ready to accept electrons. hence, it is also known as acceptor type semiconductor. The holes are majority carries and electrons are minority carriers in P-type semiconductors.

The impurities like Aluminium, Boron and other trivalent atoms have three valence electrons and same as in case of N-type semiconductor each impure atom is surrounded by four Ge (or) Si atoms.

The three valence electrons form covalent bonds with three Ge (or) Si atoms and the fourth Ge (or) Si atom has no electron to form a bond with the impure atom. So, when sufficient energy is supplied, the electron deficient bond gets the electrons from the near by bond, this way the electrons moves in one direction which is nothing but movement of hole in the reverse direction to that of electrons. In this way, hole moves and generates hole current.

Fig (1) shows the crystal lattice with one Ge atom displaced by trivalent impurity atom B.

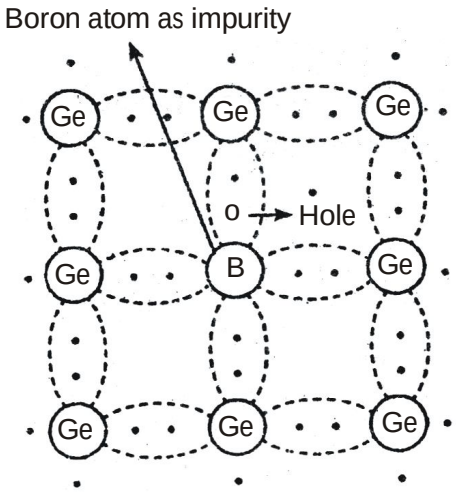



**Fig :.(1)**

Fig (2) represents the energy band description of P-type semiconductor.

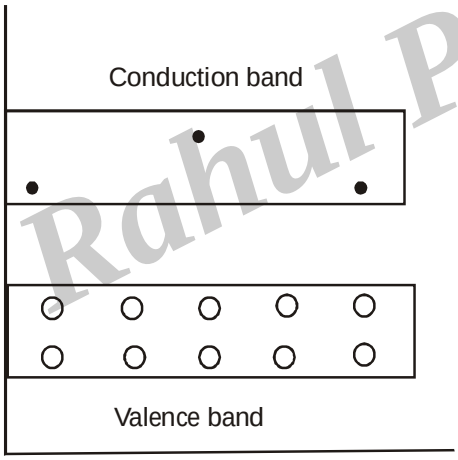



**Fig :. (2)**

It can be observed from fig (2) that with the addition of B Impurity, the number of holes in valence band is increased greatly. But few electrons are present in conduction band due to thermal energy associated with room temperature.

A P - type semiconductor is electrically neutral because the number of mobile holes is equal to the number of acceptors under all conditions.

## 1.5 Position of fermi level in Intrinsic & Extrinsic Semiconductor

**Q7. Explain position of fermi level in Intrinsic & Extrinsic semiconductor?**

*Ans :*

"Fermi level is a characteristic energy of the material". We know that in an intrinsic semiconductor there is an equal number of electrons and holes. The concentration of electrons decreases above the bottom of conduction band and similarly the concentration of holes decreases below the top of the valence band as shown in fig.

The examination of fig. shows that the centre of gravity of electrons and holes lies exactly at the middle of forbidden gap the central level is known as Fermi level.

Thus, fermi level is the energy that corresponds to the centre of gravity of the conduction electrons and holes weighted according to their energies.

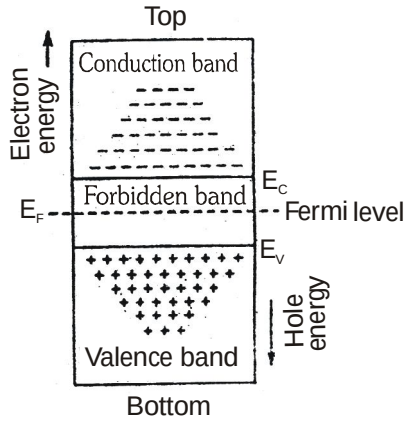



**Fig :. Showing Fermi Level**

When a donor impurity is added to an intrinsic semiconduct, it becomes N-type. Now it has more conduct ion electrons than holes as showing in fig (a)

This moves the centre of gravity up. i.e. Fermi shifts towards the conduction band.

Similarly, when an acceptor impurity is added to an intrinsic semiconductor it becomes P- type.

Now it has more holes than electrons. This shifts the Fermi level towards the valence band as shown in fig (b).

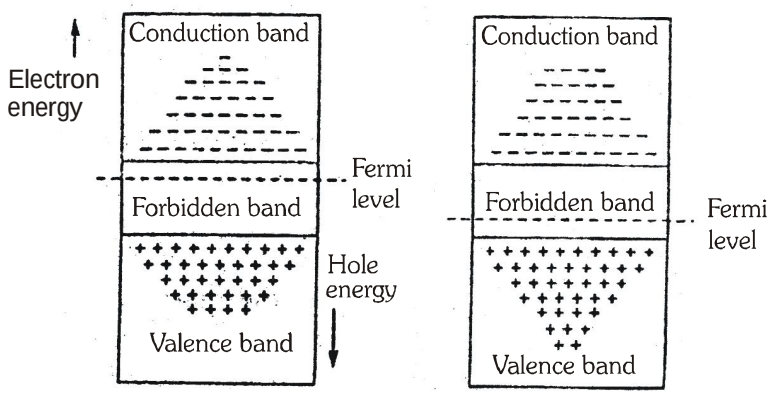



**Fig :. (a) Fermi level with donor impurity (b) Fermi level with acceptor impurity**

## 1.6 CONTINUITY EQUATION

**Q8. Derive continuity Equation?**

*Ans :*

Consider an element of volume with an area A and length dx units.

Let the average electron concentration be n and the electron current $I_n$ be function of x, at an instant t. The current entering the volume be $I_n$ and the current leaving the volume be ($I_n = dI_n$). Hence the charge is in excess which is leaving the volume.

Thus, the decrease in electrons within the volume is $\left(\frac{dI_n}{q}\right)$ and decrease in electron concentration is given by,

$$\frac{1}{qA}\frac{dI_n}{dx} = \frac{1}{q}\frac{dJ_n}{dx}$$

The rate of increase of electrons per second is $g = n_0 / \tau_n$ and rate of decrease of electrons per second is $n / \tau_n$.

Since, charge can neither be created nor destroyed, the increase in electrons per unit volume is equal to algebraic sum of all increases in electron concentration.

$$\therefore \frac{\partial n}{\partial t} = \frac{n_o - n}{\tau_n} - \frac{1}{q}\frac{\partial J_n}{\partial x}$$

The above equation is the continuity equation which represents the dynamic equilibrium in the density of electrons in a volume of semiconductor. The same equation applies for holes and is given by,

$$\frac{\partial p}{\partial t} = \frac{p_o - p}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{\partial x}$$

## 1.7 P-N JUNCTION DIODE

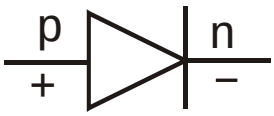
**Q9. What is junction diode ? Explain the formation of Depletion region at the junction. Explain the variation of depletion region in forward and reverse - biased condition.**

*Ans :* **(Imp.)**

**p-n junction diode**

When a p-type semiconductor is suitably joined to n-type semiconductor, a p-n junction diode is formed.

The circuit symbol of p-n junction diode is shown in figure.



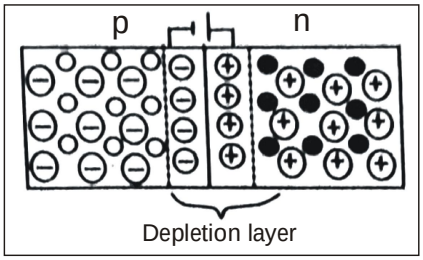

**Formation of deplection layer at the junction**

When p-n junction is formed, the free electrons on n-side diffuse over to p-side, they combine with holes and become neutral. Similarly holes on p-side diffuse over to n-side and combine with electrons become neutral.

This results in a narrow region formed on either side of the junction. This region is called depletion layer. Depletion layer is free from charge carriers.

The n-type material near the junction becomes positively charged due to immobile donor ions and p-type material becomes negatively charged due to immobile acceptor ions. This creates an electric field near the junction directed from n-region to p - region and cause a potential barrier.

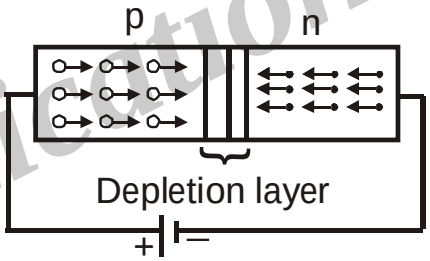
The potential barrier stops further diffusion of holes and electrons across the junction. The value of the potential barrier depends upon the nature of the crystal its temperature and the amount of doping.




**Forward bias :**

"When a positive terminal of a battery is connected to p-side and negative terminal' connected to n-side; then p-n junction diode is said to be forward biased".

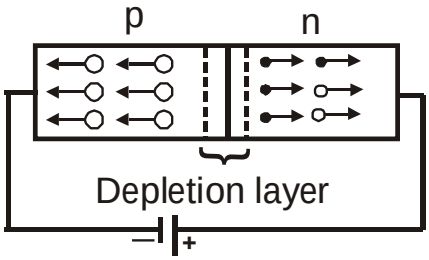
The holes in the p-region are repelled by the positive polarity and move towards the junction. Similarly electrons in the n-region are repelled by the negative polarity and move towards the junction.




As a result, the width of the depletion layer decreases. The charge carriers cross the junction and electric current flows in the circuit.

Hence in forward bias resistance of diode is low. This position is called switch on position.

**Reverse bias**




"When the negative terminal of the battery is connected to p-side and positive terminal of the battery is connected, to n-side, then the p-n junction diode is said to be reverse biased".

The holes in the p-region are attracted towards negative polarity and move away from

junction. Similarly the electrons in the n-region are attracted towards positive polarity and move away from the junction.

So, width of the depletion layer and potential barrier increases. Hence resistance of p - n junction mode increases. Thus the reverse biased diode is called switch off position.

## 1.8 RECTIFICATION

**Q10. Explain Rectification ?**

*Ans :*

Rectification is the process by which an alternating supply voltage is converted into direct supply voltage. Accordingly, a rectifier is a device which delivers a direct (unidirectional) current when connected in a suitable fashion to a source of alternating voltage. Thus it is used to change an alternating voltage into a direct one.

Vacuum diode and P-N junction diode both serve as excellent rectifiers. A junction diode allows a current to flow through it when if is forward biased. This property of diode is used for rectification.

## 1.9 HALF WAVE RECTIFIER

**Q11. Explain and derive the Expression for Half wave Rectifier with neat sketches?**

*Ans :* **(Imp.)**

Fig. a depicts the rectifying action of a semiconductor diode. The AC. voltage to be rectified is connected to the primary coil P of the power transformer, T. One end of the Secondary s of the transformer is connected to P-region of diode D while its another end is connected to N-region a load resistance R.

**Working of the rectifier**

During the first half cycle of A.C., one end of the secondary, say A, becomes positive. Then the diode D is forward biased and hence current flows through the load R in the direction of arrows. (Fig a). During the next half cycle, the end A becomes negative and consequently, the diode D is reverse biased. Therefore, no (negligible) current flows through the load R. Thus we get a unidirectional current across R. Which flows in the form of half sine waves separated by a period of $\pi$ radians, as shown by the side of Fig a.

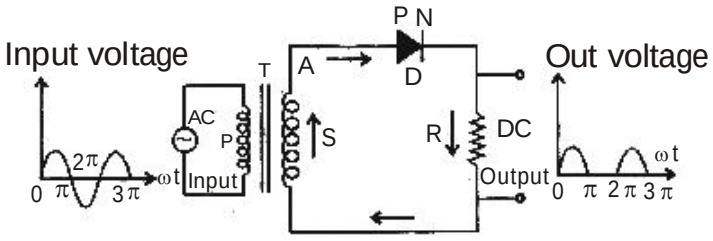



**Fig.: a**

**Mathematical Analysis**

Let the input voltage applied to the P-N junction diode in series with load R be given by

$$E = E_0 \sin \omega t$$

Then, the instantaneous output current through the load resistance R is given by

$$I = \frac{E_0 \sin\omega t}{R_f + R} = I_0 \sin\ \omega t \text{ when } 0 \le wt \le \pi$$

and $I = 0$ when $\pi \le \omega t \le 2\pi$

Where $R_f$ is the dynamic forward resistance of the semiconductor diode and

$$I_0 = \frac{E_0}{R_f + R}$$

is the peak value of the current

**(i) D.C. (average) value of output current.**

The average d.c. current over one complete cycle is given by

$$I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I.d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_0 \sin\omega t.d(\omega t) + \int_{\pi}^{2\pi} 0.d(\omega t)\right]$$

$$= \frac{I_0}{2\pi}\left[-\cos\omega t\right]_0^{\pi} = \frac{I_0}{\pi}$$

$$\therefore \quad I_{dc} = \frac{I_0}{\pi} = \frac{E_0}{\pi(R_f + R)} \qquad \text{..... (1)}$$

The d.c. (or average) output voltage across the load is given by

$$E_{dc} = I_{dc} \times R$$

$$= \frac{I_0 R}{\pi} = \frac{E_0 R}{\pi(R_f + R)}$$

**(ii) R.M.S (effective) value of output current.**

The root mean square value of the current, by definition, is given by

$$I_{rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} I^2 d(\omega t)\right]^{1/2}$$

$$= \left[\frac{1}{2\pi}\left\{\int_0^{\pi} I_0^2 \sin^2\omega t d(\omega t) + \int_{\pi}^{2\pi} 0.d(\omega t)\right\}\right]^{1/2}$$

$$= \left[\frac{1}{2\pi}\int_0^{\pi} I_0^2 \sin^2\omega t d(\omega t)\right]^{1/2}$$

$$= \frac{I_0}{2} \qquad \text{..... (2)}$$

It should be noted that this value differs from the r.m.s value of a sinusoidal current which is $I_0 / \sqrt{2}$.

**(iii) Power supplied to the circuit**

The power supplied to the circuit from the a.c. source is given by

$$P_{ac} = I_{rms}^2 (R_f + R) = \frac{I_0^2}{4}(R_f + R) \qquad \text{..... (3)}$$

**(iv) Average power supplied tot he load R**

The d.c. power output across the load R is given by

$$P_{dc} = I_{dc}^2 R = \frac{I_0 R^2}{\pi^2}$$

**(v) Rectifier efficiency**

The efficiency of rectification $\eta$ with which the half wave rectifier converts a.c. power into d.c. is defined as the ratio of d.c. output power to the total a.c. power supplied to the rectifier.

Thus,

$$\eta = \frac{\text{d.c. power supplied to load}}{\text{Total input a.c. power}} \times 100\%$$

or $$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

$$= \frac{I_0^2 R / \pi^2}{I_0^2 (R_f + R)/4} \times 100\%$$

$$= \frac{4R}{\pi^2(R_f + R)} \times 100\%$$

$$= \frac{400}{\pi^2} \cdot \frac{1}{\left[1 + \frac{R_f}{R}\right]}\% = \frac{40.6}{1 + \frac{R_f}{R}}\%$$

If $R_f << R$, the efficiency is maximum. The the oritical maximum efficiency is obtained when $R_f/R = 0$ and is equal to 40.6% only.

**(vi) Ripple factor**

The output of a rectifier contains unidirectional (d.c.) current as well as a part of a.c. A measure of a a.c. components is given by the ripple factor r which is defined as

$$r = \frac{\text{r.m.s value of all a.c. components of the output}}{\text{Average or d.c. component of the output}} = \frac{I^1_{rms}}{I_{dc}}$$

From a.c. circuit theory, the r.m.s value of the total output current $I_{rms}$, the average or d.c. value of the current $I_{dc}$ and the r.m.s. value of the a.c. components of the output $I'_{rms}$ are related by

$$I^2_{dc} + I'^2_{rms} = I^2_{rms}$$

or $$1 + \frac{I'^2_{rms}}{I_{dc}} = \frac{I^2_{rms}}{I^2_{dc}}$$

or $$\frac{I'_{rms}}{I_{dc}} = \sqrt{\left[\frac{I^2_{rms}}{I^2_{dc}} - 1\right]}$$

$$\therefore \text{ Ripple factor } r = \frac{I'_{rms}}{I_{dc}} = \sqrt{\left[\frac{I^2_{rms}}{I^2_{dc}} - 1\right]}$$

But for half wave rectifier, using equations (1) and (2)

$$\frac{I_{rms}}{I_{dc}} = \frac{I_0/2}{I_0/\pi} = \frac{\pi}{2}$$

$$\therefore \quad r = \sqrt{\left[\frac{\pi^2}{4}\right] - 1} = 1.21$$

Thus for a half wave rectifier

$$r > 1$$

or $I'_{rms} > I_{dc}$

i.e., the a.c. component of the output exceeds the d.c. value. It indicates that half wave rectifier is a poor device for converting a.c. into d.c.

**(iv) Peak inverse voltage**

Peak inverse voltage (PIV) is defined as the maximum as the maximum reverse voltage which the rectifier has to withstand during the non-conducting period.

In a half wave rectifier, the reverse voltage across the diode during non-conducting period equals the maximum transfer voltage $E_0$ across the secondary. Thus

$$PIV = E_o$$

**(viii) Voltage regulation**

Voltage regulation is the ability of a rectifier to maintain a specified output voltage irrespective of the variation in the load resistance. Since in a half wave rectifier

$$I_{dc} = \frac{I_0}{\pi} = \frac{E_0}{\pi(R_f + R)}$$

$$\text{(or) } I_{dc}(R_f + R) = \frac{E_0}{\pi}$$

$$I_{dc} R = \frac{E_0}{\pi} - I_{dc} R_f$$

$$\text{(or) } E_{dc} = \frac{E_0}{\pi} - I_{dc} R_f$$

When $I_{dc} = 0$, $E_{dc}$ has its maximum value $E_0 / \pi$. As $I_{dc}$ increases, $E_{dc}$ decreases linearly depending on the value of $R_f$. Therefore, voltage regulation of a half wave rectifier is poor.

## 1.10 P - N - Junction Full wave Rectifier

**Q12. Explain & Derive the Expressions for Full wave Rectifier ?**

*Ans :* **(Imp.)**

Fig (a) shows the circuit of centre tap full wave - rectifier employing two P-N junction diodes $D_1$ and $D_2$. The P-regions of the diodes are connected to the ends A and B of the secondary of the power transformer, the middle point of which is tapped at C and connected to the junction of N-regions through the load resistance R.

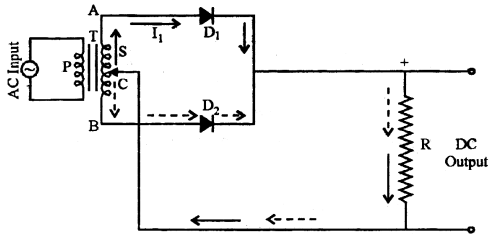



**Fig.: (a)**

**Working of the rectifier**

During the positive half -cycle of secondary voltage, one end of the secondary say, A, becomes positive and end B becomes negative. Consequently, the diode $D_1$ is forward biased and a current $I_1$ flows

in the circuit in the direction $AD_1RCA$ shown by solid arrows. During this time the diode $D_2$ is reverse biased and hence no current flows through it.

During the negative half cycle of AC input , end A becomes negative and end B positive. Consequently diode $D_2$ is forward biased and a current $I_2$ flows in the circuit through the diode $D_2$ along $BD_2RCB$ as shown by the dotted arrows. During this period, $D_1$ is reverse biased and hence does not conduct.

Thus the diodes $D_1$ and $D_2$ conduct alternately but each time the current through the load R flows in the same direction. Consequently, the resulting output current is unidirectional and flows in the form of half sine waves without separation as shown in Fig. (iii), fig b (i & ii) give the input wave forms of two diodes $D_1$ and $D_2$.

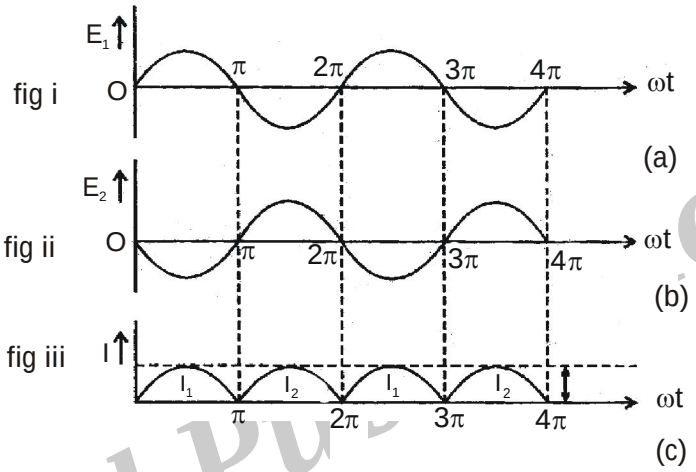



**Fig. (b)**

**Mathematical analysis**

Under the action of the sinusodial a.c. voltage of frequency $\frac{\omega}{2\pi}$ applied to the primary of the transformer, the a.c. voltage across AC and BC are given by

$E_1 = E_0 \sin \omega t$

$E_2 = E_0 \sin (\omega t - \pi)$

Where $E_0$ is the peak value of the voltage.

The corresponding current pulses in the two diodes are given by

$$\left.\begin{aligned} I_1 &= \frac{E_0}{R_f + R} \sin \omega t = I_0 \sin \omega t \\ I_2 &= 0 \end{aligned}\right\} \text{when } 0 < \omega t < \pi$$

and $I_1 = 0$

$$\left.I_2 = -\frac{E_0}{R_f + R} \sin gwt = -I_0 \sin \omega t\right\} \text{When } \pi < \omega t < 2\pi$$

where $R_f$ is the dynamic forward resistance of semiconductor diode.

**(ii) D.C. (average) value of output current**

Since the current $I_1$ and $I_2$ are of the same form ($I = I_0 \sin \omega t$), the average or d.c. value of current can be obtained by integrating the current expression between 0 and $\pi$ and dividing by the period by the period $\pi$, i.e.,

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} I.d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_0 \sin \omega t d(\omega t)$$

or $$I_{dc} = \frac{2I_0}{\pi}$$

The d.c. (or average) output voltage across the load R is,

therefore,

$$E_{dc} = I_{dc} \times R = \frac{2I_0 R}{\pi} = \frac{2R}{\pi}.\frac{E_0}{(R_f + R)} \quad \text{..... (2)}$$

**(ii) R.M.S (effective) value of load current**

The rms value of total output current is given by

$$I_{rms} = \left[\frac{1}{2\pi}\left\{\int_0^{\pi} I_0^2 \sin^2 \omega t.d(\omega t) + \int_{\pi}^{2\pi} I_0^2 \sin^2 \omega t.d(\omega t)\right\}\right]^{1/2} = \frac{I_0}{\sqrt{2}} \text{ ..... (3)}$$

**(iii) Power Supplied to the circuit**

The a.c. power input to the rectifier from the supply is given by

$$P_{ac} = I_{rms}^2 (R_f + R) = \frac{I_0^2}{2}(R_f + R) \quad \text{..... (4)}$$

**(iv) Average power supplied to the load R.**

The d.c. power output across the load R is given by

$$P_{dc} = I_{dc}^2 R = \left(\frac{2I_0}{\pi}\right)^2 .R = \frac{4I_0^2}{\pi^2}.R \quad \text{..... (5)}$$

**(v) Frequency components of rectifier output**

The output current of a full wave rectifier can be analyzed by means of Fourier series which states that any single valued, finite and contnous periodic function, say $f(\omega t)$, can be represented by the sum of such simple harmonic terms whose frequency are multiples of the frequency of the given periodic function. Thus

$$f(\omega t) = A_0 + A_1 \cos \omega t + A_2 \cos 2\omega t + .....$$
$$+ B_1 \sin \omega t + B_2 \sin 2\omega t + .....$$

(or) $$f(\omega t) = A_0 + \sum_{k=1}^{\infty} A_k \cos k\omega t + \sum_{k=1}^{\infty} B_k \sin k\omega t$$

The coefficients appearing in the series (known as Fourier constants) are given by the integrals

$$A_0 = \frac{1}{2\pi}\int_0^{2\pi} f(\omega t)$$

$$A_k = \frac{1}{\pi}\int_0^{2\pi} f(\omega t)\cos k\omega t.d(\omega t)$$

and $$B_k = \frac{1}{\pi}\int_0^{2\pi} f(\omega t)\sin k.\omega t.d(\omega t)$$

Taking $f(\omega t) = I_0 \sin \omega t$, we can calculate the values of $A_0$, $A_k$ and $B_k$. In the case of a full wave rectifier, I is positive for $\omega t = 0$ to $\omega t = \pi$ and also for $\omega t = \pi$ to $\omega t = 2\pi$, i.e.,

$I = I_0 \sin \omega t$ for $\omega t = 0$ to $\omega t = \pi$

and $I = -I_0 \sin \omega t$ for $\omega t = \pi$ to $\omega t = 2\pi$

because $\sin \omega t$ is negative in the range $\omega t = \pi$ to $\omega t = 2\pi$.

Therefore,

$$A_0 = \frac{1}{2\pi}\left[\int_0^{\pi} I_0 \sin \omega t.d(\omega t) + \int_{\pi}^{2\pi} -I_0 \sin \omega t.d(\omega t)\right]$$

$$= \frac{I_0}{2\pi}\left[\left(-\cos \omega t\right)_0^{\pi} - \left(-\cos \omega t\right)_{\pi}^{2\pi}\right]$$

$$= \frac{I_0}{2\pi}\left[(1+1)+(1+1)\right] = \frac{2I_0}{\pi}$$

Similarly,

$$A_k = \frac{1}{\pi}\left[\int_0^{\pi} I_0 \sin \omega t \cos k\omega t.d(\omega t) + \int_{\pi}^{2\pi} -I_0 \sin \omega t \cos k\omega t.d(\omega t)\right]$$

$$= \frac{I_0}{2\pi}\left[\int_0^{\pi}\left\{\sin(k+1)\omega t - \sin(k-1)\omega t\right\} d(\omega t) - \int_{\pi}^{2\pi}\left\{\sin(k+1)\omega t - \sin(k-1)\omega t\right\} d(\omega t)\right]$$

$$= \frac{I_0}{2\pi}\left[-\cos\frac{(k+1)\omega t}{k+1} + \cos\frac{(k-1)\omega t}{k-1}\right]_0^{\pi} - \frac{I_0}{2\pi}\left[-\cos\frac{(k+1)\omega t}{k+1} + \cos\frac{(k-1)\omega t}{k-1}\right]_{\pi}^{2\pi}$$

or $A_k = 0$, when k is odd.

But when k is even

$$A_k = \frac{I_0}{2\pi}\left[\frac{2}{k+1} - \frac{2}{k-1}\right] - \frac{I_0}{2\pi}\left[-\frac{2}{k+1} + \frac{2}{k-1}\right]$$

$$= \frac{I_0}{2\pi}\left[\frac{2}{k+1}-\frac{2}{k-1}\right] = -\frac{4I_0}{\pi\left(k^2-1\right)}$$

Again,

$$B_k = \frac{1}{\pi}\left[\int_0^{\pi} I_0 \sin\omega t \sin k\omega t.d(\omega t) + \int_{\pi}^{2\pi} -I_0 \sin\omega t \sin k\omega t.d(\omega t)\right]$$

$$\text{or } B_k = \frac{I_0}{2\pi}\left[\int_0^{\pi}\{\cos(k-1)\omega t - \cos(k+1)\omega t\}\,d(\omega t) - \frac{I_0}{2\pi}\int_{\pi}^{2\pi}\{\cos(k-1)\omega t - \cos(k+1)\omega t\}\,d(\omega t)\right]$$

$$= \frac{I_0}{2\pi}\left[\sin\frac{(k-1)\omega t}{k-1} - \sin\frac{(k+1)\omega t}{k+1}\right]_0^{\pi} - \frac{I_0}{2\pi}\left[\sin\frac{(k-1)\omega t}{k-1} - \sin\frac{(k+1)\omega t}{k+1}\right]_{\pi}^{2\pi}$$

= 0, for all values of k.

Thus the output current I can be expressed in the form of a Fourier series as

$$I = f(\omega t) = \frac{2I_0}{\pi} - \sum_{k=even}^{\infty}\frac{4I_0}{(k^2-1)}\cos\omega t$$

$$= \frac{2I_0}{\pi} - \frac{4I_0}{3\pi}\cos 2\omega t - \frac{4I_0}{15\pi}\cos 4\ \omega t \qquad \ldots\ldots (6)$$

Thus the output current of a full wave rectifier has a d.c. component $\frac{2I_0}{\pi}$ and a series of a.c. components (even harmonics only) or ripples. The first harmonic frequency (or fundamental) term is absent and the lowest frequency term has an angular frequency of $2\omega$

**(vi) Rectifier Efficiency**

In a rectifier, the useful power output is the d.c. power which is developed across the load R.

Therefore, efficiency

$$\eta = \frac{\text{d.c. power supplied to the load}}{\text{Total input a.c.power}} \times 100\%$$

$$= \frac{P_{dc}}{P_{ac}} \times 100\% = \frac{4I_0^2R/\pi^2}{I_0^2(R_f+R)/2} \text{ Using Eqns (4) \& (5)}$$

$$\text{or } \eta = \frac{8}{\pi^2}.\frac{1}{1+\frac{R_f}{R}} \times 100\% = \frac{81.2}{1+\frac{R_f}{R}}\% \qquad \ldots\ldots\ldots (7)$$

The efficiency is maximum when $\frac{R_f}{R}$ = 0 and is equal to 81.2%. It is thus double that of a half wave rectifier.

**(vii) Ripple factor**

The ripple factor is given by

$$r = \frac{I'_{rms}}{I_{dc}} = \sqrt{\left[\frac{I^2_{rms}}{I^2_{dc}} - 1\right]}$$

Using eqns (1) and (3)

$$\frac{I_{rms}}{I_{dc}} = \frac{I_0/\sqrt{2}}{2I_0/\pi} = \frac{\pi}{2\sqrt{2}}$$

$$\therefore \text{ Ripple factor } r = \sqrt{\left[\left(\frac{\pi^2}{B}\right) - 1\right]} = 0.48$$

Thus the d.c. output voltage of the full wave rectifier has a smaller ripple.

**(viii) Peak inverse voltage**

As already defined, PIV is the maximum reverse voltage which the rectifier has to with stand during the non conduction period.

In the case of a full wave rectifier, if the diode $D_1$ is conducting and $D_2$ non conducting point C is positive w.r.t. point B and both $E_1$ and $E_2$ are passing through their maximum values.

If the voltage drop across $D_1$ is, neglected, voltage developing across R will be $E_0$ with upper end positive w.r.t C. Thus the reverse voltage appearing across diode $D_2$

PIV = P.D. across R – ($-E_0$)

= $E_0 + E_0 = 2E_0$

thus in a full wave rectifier, PIV across each diode is two times the maximum transformer voltage measured from the centre - tap to either end.

**(ix) Voltage regulation**

Good voltage regulation means that the output remains constant. It is expressed as a percentage and is given by

$$\text{voltage regulation} = \frac{(E_0 - E_L) \times 100}{E_L}\%$$

Where $E_0$ = output voltage without load

and $E_L$ = output voltage at full load

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**Q13. Distinguish between Half & Full wave rectifiers?**

*Ans :*

(1) Compared to half wave circuit, the full wave circuit has less ripple and is more easily filtered owing to the higher ripple frequency.

(2) Rectification efficiency of a full wave rectifier is twice that of half wave rectifier.

(3) Full wave rectifiers can supply a large load current as compared to half wave rectifiers.

(4) For the same d.c. output voltage, the transformer secondary voltage required in full wave rectifier is twice that of required for half wave rectifier.

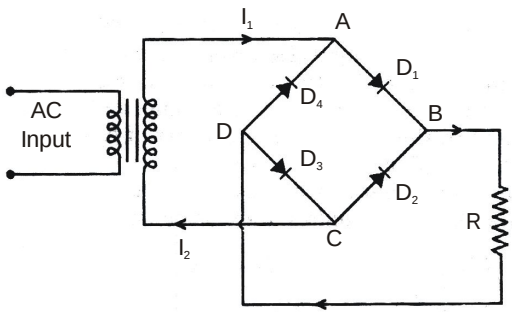
(5) The half wave rectifier, however, has the advantages of simplicity and is less costly.

## 1.11 Bridge Type Full wave Rectifier

**Q14. Explain about Bridge type full wave rectifier? and give advantages & disadvantages?**

*Ans :*

An important rectifier circuit arrangement is the bridge rectifier or double way rectifier shown in Fig. It is known so because in this circuit the four PN junction diodes $D_1$, $D_2$, $D_3$ and $D_4$ are arranged in the form of four resistances of wheatstone Bridge network. The two opposite ends A and C of the network are connected to the ends $S_1$ and $S_2$ of




**Fia.: (a)**

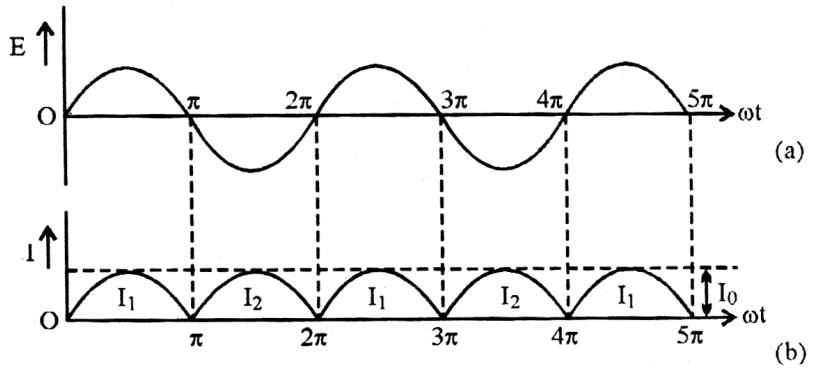
the secondary of transformer while the ends B and D are connected to the load resistance R.

**Working of the rectifier**

Under the action of an a.c. voltage applied to the primary of the transformer, the voltage across the secondary is given by

$E_1 = E_0 \sin \omega t$

Which varies with $\omega t$ as shown in Fig (b)



In the half cycle in which the potential of the transformer has a polarity such that A is positive and C is negative diode $D_1$ and $D_3$ are forward biased and conduction takes place via diode $D_1$, load resistance R and diode $D_3$.

Consequently, a current $I_1$ flows in the direction $ABRDCS_2S_1A$ as shown in Fig (a). On the other half cycle when the terminal C is positive with respect to A, diodes $D_2$ and $D_4$ are forward biased. Therefore, conduction takes place via the diodes $D_2$ and $D_4$ and a current $I_2$ flows in the direction $CBRDAS_1S_2C$. Same process is repeated in the subsequent half cycles of the a.c. input. However, the current through the load R flows in the same direction in both the halves of the applied a.c. voltage. Thus the current is unidirectional, and the wave shape of the current in the load is similar to that of full wave rectifier, as shown in Fig (b).

In this evident that two diodes conduct simultaneously in series.

Therefore, the current pulses are represented by

$$\left.\begin{aligned} I_1 &= \frac{E_0}{2R_f + R}\sin\omega t = I_0 \sin\omega t \\ I_2 &= 0 \end{aligned}\right\} \text{ where } 0 < \omega t < \pi$$

$$\text{and } \left.\begin{aligned} I_2 &= \frac{E_0}{2R_f + R}\sin\omega t = -I_0 \sin\omega t \\ I_1 &= 0 \end{aligned}\right\} \text{ when } \pi < \omega t < 2\pi$$

Where $R_f$ is the dynamic forward resistance of each diode and $I_0$ the maximum current given by

$$I_0 = \frac{E_0}{2R_f + R}$$

The expression for average d.c. current $\left[= \frac{2I_0}{\pi}\right]$, r.m.s value of current $(= I_0 / \sqrt{2})$ and the ripple factor (=0.48) are the same as in case of centre tap full wave rectifier but the efficiency is given by

$$\eta = \frac{81.2}{1 + \frac{2R_f}{R}}\%$$

The peak inverse voltage in case of bridge rectifier is the voltage across each diode and is equal to $E_0$, the maximum voltage across the secondary of the transformer.

**Advantages**

(i) As the transformer secondary winding is fully utilized centre top of the secondary is not required. It reduces the transformer cost in bridge rectifier.

(ii) The peak inverse voltage across each diode is a bridge rectifier is one half as that of a centre tap full wave rectifier for the same d.c. output.

(iii) Since the current in both the primary and secondary of the transformer flow for the entire cycle, a smaller transformer can be used.

**Disadvantages.**

(i) Two extra diodes are required in the circuit.

(ii) As the diodes are used in series, there is a larger voltage drop across the diodes. It results in poor rectification efficiency and poor voltage regulation.

## 1.12 ZENER DIODE

**Q15. What is zener diode and explain VI characteristics of zener diode?**

*Ans :*

Zener diode is a reverse based heavily doped semiconductor (silicon or germanium) PN junction diode.

Which is operated exclusively in the breakdown region. The symbol of a Zener diode is shown in Fig a. For normal operation of a Zener diode, in breakdown region, the current through the diode should be limited by an external circuit. Hence the power V dissipated across the junction is within its power-handling capacity. Unless this precaution is observed, a large current will destroy the diode.

Figa shows symbol for Zener diode

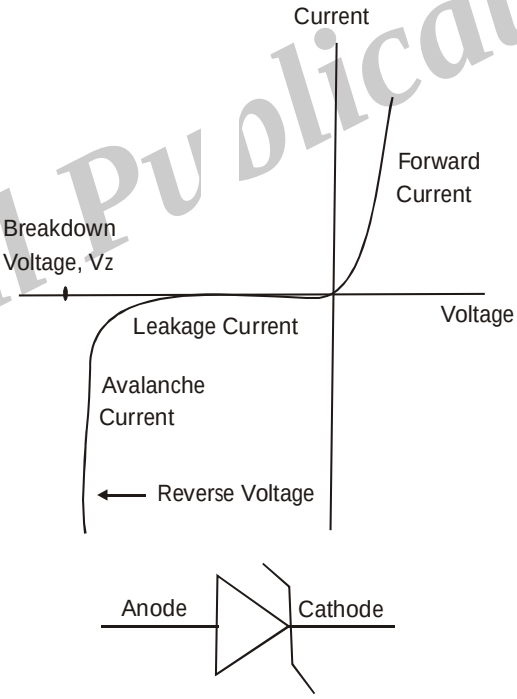



**Fig.: Zener Diode V - I Characteristics Curve**

**V-I characteristics:**

The V-I characteristic curve for the Zener diode is shown in fig. It can be seen from the figure, that, as the reverse voltage applied Fig b, to the PN junction is increased, at a particular voltage, the current increases enormously from its normal cut off value. This voltage is called zener voltage or breakdown voltage (V).n is increased, at a particular voltage, the current increases enormously from its normal cut off value. This voltage is called zener voltage or breakdown voltage (V).

## 1.13 ZENER DIODE AS VOLTAGE REGULATOR

**Q16. Explain zener Diode as Voltage Regulator?**

*Ans :*

A Zener diode is an ordinary P-N junction diode except that it is properly doped so as to have a very sharp and almost vertical breakdown. It is exclusively operated under reverse bias conditions. Typical current - voltage characteristics for such a diode are shown in Fig (a). It may be seen from the characteristics that when forward biased, its

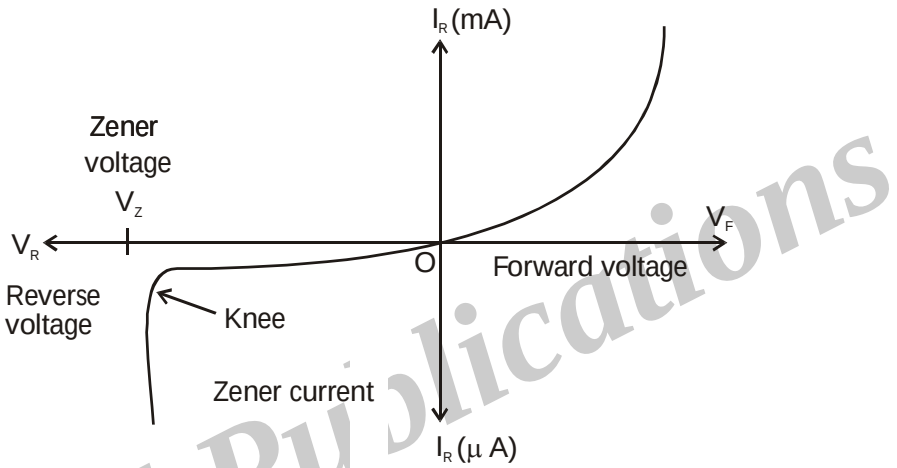



**Fig.: (a)**

Characteristics are just that of an ordinary semiconductor diode. when reverse biased, a small reverse saturation current flows through it which remains approximately constant until a certain critical voltage, called break down voltage, is reached. Beyond this voltage, the reverse current $I_R$ increases sharply to a high value. The break down voltage $V_Z$ is called the Zener voltage and the reverse current as Zener current.

Thus, when a Zener diode is operated in the break down region, the voltage across the diode remains almost constant (equal to $V_Z$) for the large changes of the reverse current. The voltage across a Zener diode thus serves as a reference and the diode is used as a voltage reference device for stabilizing a voltage at a predetermined value.

### Circuit Details

A simple Zener diode voltage stabilizer circuit is shown in Fig (b) . This circuit is used to maintain a constant voltage across a load resistor $R_L$ inspite of variations in either the supply voltage or the load current (due to a change in the load resistance) or both.

In the circuit, the input is a d.c. voltage whose voltage variations are to be regulated. The P-junction of the Zener diode is connected to the negative point of the input voltage and N-junction to the positive.

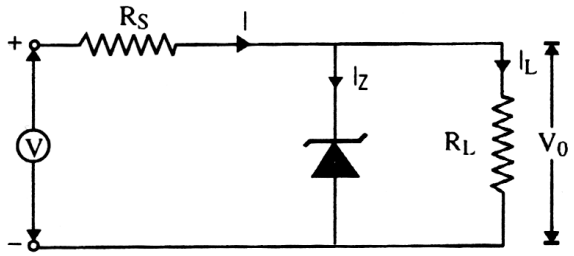



**Fig.: (b)**

Thus the Zener diode is reverse biased. The value of the series resistor $R_S$ is so chosen that initially the diode operates in the breakdown region.

**Operation:**

Let I be the current drawn from the supply source, $I_Z$ the current through the Zener diode and $I_L$ that across the load resistance $R_L$. Then kirchoffs law give

$$I = I_Z + I_L \quad \text{..... (1)}$$

$$V_0 = V - IR_S \quad \text{.....(2)}$$

and $$V_0 = I_L R_L \quad \text{..... (3)}$$

**Case I**

When supply voltage V remains constant and load resistance $R_L$ varies

Since the output voltage $V_0$ tends to remain constant, then eq. (2) gives

$\delta T = 0$ (because V and $R_S$ are constant)

Then eq. (1) gives

$$\delta I = \delta I_Z + \delta I_L = 0$$

or $$\delta I_Z = -\delta I_L$$

Thus, if the load resistance increases, when the supply voltage is fixed, the load current $I_L$ decreases and the Zener diode current $I_Z$ increases by equal amount. Thus the voltage $V_o$ across the load will tend to remain constant.

**Case II**

When load resistance remains constant, the total constant I and the Zener current $I_Z$ change equally to keep the load current $I_L$ constant. Thus if total current I decreases by $\delta I$, the diode current $I_Z$ also decreases by the same amount, so that load current $I_L$ remains constant and the voltage $V_0$ across the load will tend to remain constant.

## PROBLEMS

**1. A half wave rectifier uses a transformer of turns ratio 8: 1. If the primary voltage is 230 V (rms), find**

**(i) d.c. output voltage**

**(ii) peak inverse voltage**

*Sol :*

Given, R.M.S. primary voltage = 230 Volt

$\therefore$ Maximum primary voltage

$$E_p = \sqrt{2} \times \text{r.m.s. primary voltage}$$

$$= \sqrt{2} \times 230 = 324.3 \text{ Volt}$$

Since primary to secondary turn ratio

$$\frac{N_1}{N_2} = 8$$

$\therefore$ Maximum secondary voltage

$$E_s = E_p \times \frac{N_1}{N_2} = 324.3 \times \frac{1}{8}$$

$$= 40.54 \text{ Volt}$$

**(i) d.c. output voltage**

$$E_{dc} = I_{dc} \times R = \frac{I_0}{\pi} \times R$$

$$= \frac{E_s}{\pi} = \frac{40.54}{3.14} = 12.9 \text{ volt}$$

**(ii) peak inverse voltage**

Since the diode is reverse biased during the negative half cycle of a.c. supply, it conducts no current. Therefore, maximum transformer secondary voltage appears across the diode. Hence peak inverse voltage.

PIE = $E_i$ = **40.54 volt**

**2. A full wave rectifier uses a centre-tapped transformer. The a.c. voltage from its centre tap to either end is 10 sin 314t. The load resistance of the circuit is 40Ω and diode resistance 10Ω. Find $I_{dc}$, $I_{rms}$ ripple factor and rectifier efficiency.**

*Sol :*

(i) D.C. (average) value of output centre

$$I_{dc} = \frac{2I_0}{\pi}$$

Where $I_0 = \frac{E_0}{R_f + R} = \frac{10}{10 + 40} = 0.2$ A

$$\therefore \quad I_{dc} = \frac{2 \times 0.2}{3.14} = \mathbf{0.127\ A}$$

(ii) R.M.S. value of load current

$$I_{rm} = \frac{I_0}{\sqrt{2}} = \frac{0.2}{1.41} = \mathbf{0.142\ A}$$

(iii) Ripple factor $r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

$$= \sqrt{\left(\frac{0.142}{0.127}\right)^2 - 1} = \sqrt{1.25 - 1}$$

$$= \sqrt{0.25} = \mathbf{0.5}$$

(iv) Rectifier effciency

$$\eta = \frac{81.2}{1 + \frac{Rf}{R}}\% = \frac{82.1}{1 + \frac{10}{50}}\%$$

$$= \frac{81.2}{1.2}\% = \mathbf{67.7\%}$$

---

**3. An a.c. supply of 230 volt, 50 Hz is applied to bridge type full wave rectifier circuit through a transformer of turn ration 4 : 1. Assuming the diodes to be ideal and resistance r = 200Ω, find**

**(i) d.c. output voltage**

**(ii) peak inverse voltage**

**(iii) output frequency.**

*Sol :*

Given,

Primary voltage = 230 volt

$\therefore$ R.M.S. secondary voltage

$$= 230 \times \frac{N_2}{N_1} = 230 \times \frac{1}{4} = 57.7 \text{ volt.}$$

$\therefore$ Maximum voltage across secondary

$$E_0 = 57.5 \times \sqrt{2} = 81.3 \text{ volt}$$

(i) d.c. output voltage

$$E_{dc} = I_{dc} \times R = \frac{2I_0}{\pi} R = \frac{2R}{\pi} \cdot \frac{E_0}{(R_f + R)}$$

$$= \frac{2 \times 200}{3.14} \times \frac{81.3}{200} (\because R_f = 0 \text{ for ideal diode})$$

$$= \mathbf{51.87 \text{ volt}}$$

(ii) The peak inverse voltage in case of bridge rectifier is equal to maximum secondary voltage i.e.,

$$PIV = E_0 = \textbf{81.3 volt.}$$

(iii) In full wave rectifier, for each cycle of input a.c. voltage, there are two output pulses. Therefore, output frequency is twice that of the a.c. supply frequency i.e.,

$$f_{out} = 2 \times F_{in} = 2 \times 50 = \textbf{100 Hz}$$

**4. A power supply is delivering 100 watts to a load of 10KΩ. Find voltage present across the load if the ripple factors is 0.1%.**

*Sol :*

We know that power

$$\therefore \quad P = \frac{V^2}{R}$$

where V is the voltage across load R

$$V = \sqrt{[(PR)]} = \sqrt{[(100 \text{ watt}) (10{,}000 \text{ ohms})]}$$

$$= 1000 \text{ volts}$$

Again, the ripple factor

$$r = \frac{\text{a.c. voltage}}{\text{d.c. voltage}} = \frac{0.1}{100} \text{(given)}$$

$$\therefore \quad \text{a.c. voltage} = \frac{0.1}{100} \times \text{d.c. voltage}$$

$$= 0.001 \times 1000 = \textbf{1 volt}$$

**5. A full wave rectifier with a load resistance of 15000 ohms uses an inductance filter of 15 henry. The peak value of the applied voltage is 250 volts and the frequency is 50 Hz. Calculate the d.c. load current, ripple factor and d.c. output voltage.**

*Sol :*

If $E_0$ is the peak value of the a.c. input voltage of frequency $\omega$ applied to the full wave rectifier, then the rectified output voltage of the rectifier, negleting a.c. harmonics higher than the second, is given by

$$E = \frac{2E_0}{\pi} - \frac{4E_0}{3\pi} \cos 2\omega t$$

The d.c. component of output voltage $= \frac{2E_0}{\pi}$

Therefore d.c. component of output (load) current

$$I_{dc} = \frac{E_{dc}}{R} = \frac{2E_0}{\pi R}$$

where R is the load resistance.

Given that R = 15000 ohms and $E_0$ = 250 volts.

$$\therefore \quad I_{dc} = \frac{2 \times 250}{3.14 \times 15000} = 0.0106 \text{ amp.} = \textbf{10.6 mA}$$

The d.c. output voltage

$E_{dc} = I_{dc}. R = 0.0106 \text{ amp} \times 15{,}000 \text{ ohm} = 159 \text{ volts.}$

Now peak value of the a.c. component (ripple) voltage = $\frac{4E_0}{3\pi}$

$\therefore$ r.m.s. value of ripple voltage = $\frac{1}{\sqrt{2}} . \frac{4E_0}{3\pi}$

Since the ripple frequency is $2\omega$. Hence

Impedance of filter circuit = $\sqrt{\left[R^2 + (2\omega L)^2\right]}$

Therefore, r.m.s. value of a.c. component of output current

$$I'_{rms} = \frac{1}{\sqrt{2}} . \frac{4E_0}{3\pi} . \frac{1}{\sqrt{\left[R^2 \_ (2\omega L)^2\right]}}$$

$$= \frac{4 \times 250}{1.414 \times 3 \times 3.14} \times \frac{1}{\sqrt{[(15000)^2 + (2 \times 3.14 \times 50 \times 15)^2]}}$$

$$= \frac{1000}{13.32} \times \frac{1}{17711.6}$$

$= 4.24 \times 10^{-3}$ amp $= 4.24$ mA.

Therefore, ripple factor

$$r = \frac{I'rms}{I_{dc}} = \frac{4.24}{10.6} = 0.4$$

**6. The d.c. output voltage is 40 volt at full load and 41 volt without any load any load current. Calculate the load regulation regulation factor in percent.**

*Sol :*

Regulation factor is given by

$$\text{V.R.} = \frac{E_0 - E_L}{E_L} \times 100\%$$

Here, $E_0$ = output voltage without load

= 41 volt

$E_L$ = output voltage at full load

= 40 volt

Therefore, load regulation factor in percent

$$= \frac{41 - 40}{40} \times 100\% = \frac{1}{40} \times 100\%$$

**= 2.5%**

# Short Question and Answers

**1. Explain the Introduction of Energy band?**

*Ans :*

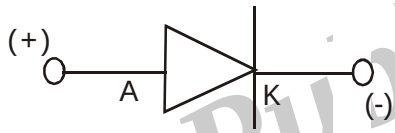
In case of solids, the atoms are arranged in a systematic space lattice and hence the atom is greatly influenced by neighbouring atoms. The closeness of atoms results in the intermining of electrons of neighbouring atoms, of course, for the valence electrons in the outermost shells which are not strongly bounded by nucleus.

Due to intermining the number of permissible energy levels increases. Hence in case of a solids, instead of single energy levels associated with the single atom, there will be bands of energy levels. A set of such closely packed energy levels is called an energy band.

**2. What is a PN Junction Diode ?**

*Ans :*

In a piece of semiconductor material if one half is doped by P-type impurity and other half is doped by N-type impurity, a PN Junction diode is formed. The plane dividing the two halves (or) zones is called PN Junction.

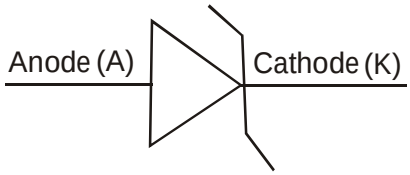



(Diagram)

**3. What is Zener diode?**

*Ans :*

Zener diode is a specially designed PN junction diode. A reverse biased heavily doped PN junction diode. A reverse biased heavily doped PN junction diode which is operated in the breakdown region is known as Zener diode. It is also called as voltage regulator diode or breakdown diode.




(Diagram)

**4. Distinguish between intrinsic and extrinsic semiconductors.**

*Ans :*

**Intrinsic semiconductor**

- A semiconductor in its pure form without impurity is called an intrinsic semiconductor
- The number of free electrons is equal to the number of holes.

- In it, electrical conductivity is the function of temperature alone
- Fermi energy level lies at the centre of forbidden energy gap.

**Extrinsic semiconductor**

- When a small amount of impurity is doped in pure semiconductor it becomes extrinsic semiconductor
- The number of free electrons and hole never equal. In n-type majority carriers are electrons. In p-type majority carriers are holes.
- In it, electrical conductivity is the function of temperature as well as concentration of impurity atoms doped in it.
- In n-type Fermi level is just below the conduction band where as in p-type Fermi energy level is just above the valance band.

**5. Distinguish between avalanche and Zenerbreakdown?**

*Ans :*

**Avalanche Breakdown**

- When both sides of the PN junction are lightly doped and the depletion layer becomes large.
- The electric field across the depletion layer is not so strong.
- Due to the collision, covalent bonds are broken and electron hole pairs are generated.
- Reverse voltage must be greater than 6V

**Zener breakdown**

- When both sides of the PN junction heavily doped and the depletion Layer is narrow
- A very strong electric field is produced across the thin depletion layer.
- Due to strong electric field, the covalent bonds breaks and large number of electrons and holes are produced.
- Reverse voltage must be less than 4V.

**6. Differentiate N-type and P-type semiconductor.**

*Ans :*

| S.No. | N-Type | P-Type |
|---|---|---|
| 1. | It is donor type | It is acceptor type |
| 2. | Impurity atom is pentavalent | Impurity atom is trivalent |
| 3. | Donor level lies close to the bottom of the conduction band. | Acceptor level lies close to the top of the valence band. |
| 4. | Electrons are the majority carriers and holes are the minority carriers. | Holes are the majority carriers and electrons are the minority carriers. |

**7. Difference between Half wave and Full wave rectifier?**

*Ans :*

**Half wave rectifier**

- A rectifier which rectifies only one half of each AC supply.
- The frequency of the output signal is exactly the same as that of the input signal.
- Half wave rectifier gives discontinuous and pulsating DC output, Half wave rectification involves a lot of wastage energy.
- Half wave rectifier is unidirectional.
- Half wave rectifier efficiency around 40.6 %.
- Half wave rectifier is only one diode is required.

**Full wave rectifier :**

- A rectifier which rectifies both halves of each AC input cycle is called as full wave rectifier
- It gives continuous and pulsating output.
- The frequency of the output signal is double that of the input signal.
- A full wave rectifier is bi-directional.
- Half wave rectifier efficiency around 81.2%.
- Full wave rectifier varies from 2 to 4, in case of a bridge rectifier.

**8. Difference between pn junction diode and zener diode?**

*Ans :*

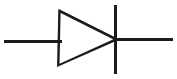
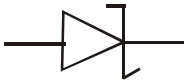
| S.No. | P-n Junction diode | Zener diode |
|---|---|---|
| 1. | The electricity flows in one direction | The electricity flows in both the direction. |
| 2. | The reverse bias permanently damages the depletion region. | The reverse bias makes the electricity flow in both the direction. |
| 3. | The width of depletion region is large because the p and n region is lightly doped. | The width of depletion region is narrow because the p and n region is heavily doped. |
| 4. | This is used for rectification. | This is used for voltage regulation. |

**9. Distinguish between conductors, semiconductors and insulators?**

*Ans :*

| S.No. | Conductors | Semiconductors | Insulators |
|---|---|---|---|
| 1. | Easily conducts the electrical current. | Conducts the electric current less than conductor and greater than insulator. | Does not conduct any current |
| 2. | Has only one valence electron in its outermost orbit. | Has four valence electron in its outermost orbit. | Has eight valence election in its outermost orbit. |
| 3. | Conductor formed using metallic bonding | Semiconductors are formed due to covalent bonding. | Insulators are formed due to ionic bonding |
| 4. | Valence and conduction bands are overlapped | Valence and conduction bands are separated by forbidden energy gap of 1.1 eV. | Valence and conduction bands are separated by forbidden energy gap of 6 to 10 eV. |
| 5. | Resistance is very small | Resistance is high | Resistance is very high |
| 6. | It has positive temperature coefficient. | It has negative temperature coefficient. | It has negative temperature coefficient |
| 7. | Ex: copper, aluminium, etc. | Ex : silicon, germanium, etc | Ex: Mica, Paper, etc |

# Choose the Correct Answer

1. Conductivity of semiconductors [ b ]
   (a) Moderate (b) High
   (c) Low (d) a & c
2. Temperature coefficient of resistance for semiconductor [ b ]
   (a) Positive (b) Negative
   (c) Neutral (d) None
3. Example for pentavalent impurity [ d ]
   (a) Bismuth (b) Antimony
   (c) Phosphorous (d) All
4. Symbol of zener diode [ c ]
   (a)  (b) 
   (c)  (d) None of the above
5. Expression for drift velocity [ c ]
   (a) $V = \frac{\mu}{\in}$ (b) $V = \frac{E}{\mu}$
   (c) $V = \mu E$ (d) $V = \frac{1}{\mu E}$
6. Efficiency of full wave rectifier [ d ]
   (a) 80% (b) 90%
   (c) 85% (d) 81.2%
7. In PN Junction diode _____ type of impurities added [ a ]
   (a) Trivalent (b) Pentavalent
   (c) Nobel gases (d) None of the above
8. A Zener diode has _____break down voltage [ a ]
   (a) Sharp (b) Zero
   (c) Undefined (d) None
9. Partial differential Equation is known as _____ [ b ]
   (a) Dis continuity Equation (b) Continuity Equation
   (c) Conductivity Equation (d) None of the above
10. PN Junction diode used as [ b ]
    (a) Voltage Regulation (b) Rectification
    (c) Regulator (d) None of the above

# Fill in the blanks

1. Lowest unfilled energy bond is known as _____
2. The separation between conduction bond and valence bond is known as _____
3. In case of P-type semiconductors _____ impurity is added to a pure crystal.
4. The force electrons move from negative to positive terminal with steady velocity constitutes current is known as _____
5. When electrons from N-side crosses over to P-side where they combine and vice versa become neutral, this region is known as _____
6. A semiconductor in a extremely pure form is known as _____
7. Ripple factor is defined as ratio of _____
8. Form factor is defined as ratio of _____
9. Maximum passible voltage across a diode when it is reverse biased is _____
10. The value of ripple factor for full wave bridge rectifier _____

## ANSWERS

1. Conduction bond
2. Forbidden energy gap
3. Trivalent
4. Drift current
5. Depletion region
6. Intrinsic semiconductor
7. $\left[\frac{\text{rms value of ac compound}}{\text{d.c. value of wave}}\right]$
8. Peak inverse voltage
9. Peak inverse voltage
10. 0.48

UNIT II

**Bipolar Junction Transistor (BJT)**

p-n-p and n-p-n transistors, current components in transistors, CB, CE and CC configurations - transistor as an amplifier - RC coupled amplifier - Frequency response (Qualitative analysis).

**Feedback concept & Oscillators**

Feedback, General theory of feedback - Concepts of oscillators, Barkhausen's criteria, Phase shift oscillator - Expression for frequency of oscillation.

## 2.1 P-N-P & N-P-N TRANSISTORS

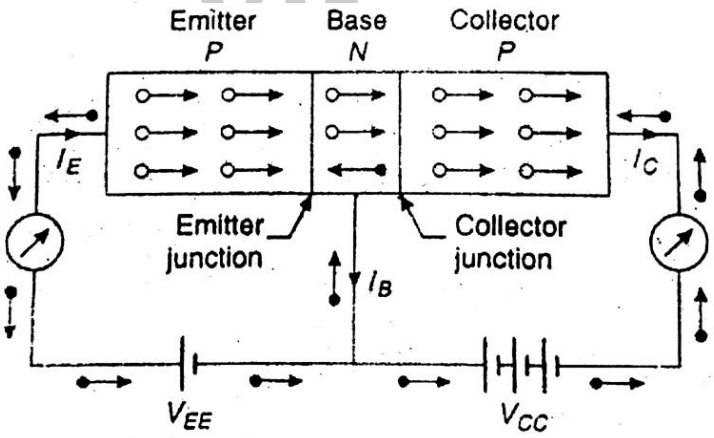
**Q1. Explain about Bipolar junction transistor and its types ?**

*Ans :* **(Imp.)**

A junction transistor is simply a sandwich of one type of semiconductor material between two layers of the other type. Accordingly, there are two types of transistors:

1. N-P-N transistor
2. P-N-P transistor

When a layer of P-type material is sandwiched between two layers of N-type material, the transistor is known as N-P-N transistor. This is shown in fig 3.1 (a) similarly, when a layer of N-type material is




**Fig(a). : Operation of PNP Transistor**

Sandwiched between two layers of P-type material, the transistor, is known as P-N-P transistor. This is shown in fig (a). Transistors are made either from silicon or germanium crystal. The symbols employed for N-P-N and P-N-P transistors are also shown in fig (a)

Although the two outer regions are of the same type but they cannot be interchanged. The reason is that the two regions have different physical and electrical properties. The collector region is made physically larger than emitter region. The base is very thin and lightly doped. The emitted is heavily doped while the doping of collector is between the heavy doping of emitter and light doping of the base.

A transistor (N-P-N or P-N-P) has the following sections.

**(i) Emitter**

This form the left hand section of the transistor. The main function of this region is to supply majority charge carriers (either electrons or holes) to the base and hence it is more heavily doped in comparison to other regions.

**(ii) Base**

The middle section of the transistor is known as base. This is very lightly doped and is very thin ($10^4$ m) as compared to either emitter or collector so that it may pass most of the injected charge carriers to the collector.

**(iii) Collector**

The right hand section of the transistor is called as collector. The main functions the collector is to collect majority charge carriers through the base. This is moderately doped.

As regards the symbols, arrow head is always at the emitter. The direction indicates the conventional direction of current flow, i.e. in case of N-P-N transistor it is from base to emitter (base is positive with respect to emitter) while in case of P-N-P transistor it is from emitter to base (emitter is positive with respect to base).

### 2.1.1 P-N-P Transistor

**Q2. Explain the operation of P-N-P transistor?**

*Ans :* **(Imp.)**

P-N-P transistor with emitter base junction as forward biased and collector-base junction as reverse biased. The operation of P-N-P transistor is as follows

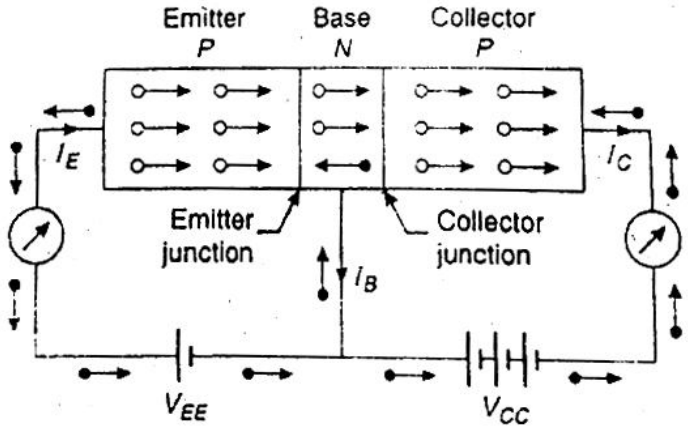



**Fig. : Operation of PNP transistor**

The holes of P region (emitter) are repelled by the positive terminal of battery $V_{EE}$ towards the base. The potential barrier at emitter junction is reduced as it is forward biased and hence the holes cross this junction and penetrate into N-region. This constitutes the emitter current $I_E$. The width of the base region is very thin and it is lightly dropped and hence only two to five percent of the holes recombine with the free electrons of N-region. This constitute the base current $I_E$, which of course, is very small. The remaining holes (95'6 to 98%) are able to drift across the base and enter the collector region. They are swept up by the negative collector voltage $V_{CC}$. They constitute the collector current $I_C$.

As each hole reaches the collector electrode, an electron is emitted from the negative terminal of battery and neutralizes the hole. BNow, a covalent bond near the emitter electrode breaks down. The liberated electron enters the positive terminal of battery $V_{EE}$ while the hole immediately moves towards the emitter junction. This process is repeated again and again. Here it should be remembered that :

(i) Current condition within PNP transistor takes place by hole conduction from emitter to collector, i.e., majority charge carriers in a PNP transistor are holes. The conduction in the external circuit is carriers out by electrons.

(ii) The collector current is slightly less than the emitter current. This is due to the fact that 2 to 5% of the holes are lost in recombination with electron in base region. Thus, the collector current is slightly less than emitter current.

(iii) The collector current is a function of emitter current, i.e, with the increase or decrease in the emitter current, a corresponding change in collector current is observed.

Besides the hole current, there is electron current which flows from base region to emitter region. This current depends upon emitter base potential. As the width of the base region is very small, the ratio of hole current to electron current is very small. So for all practical purposes, the electron current may be neglected.

Thus, only the hole current plays an important rol.e in the operation of PNP transistor.

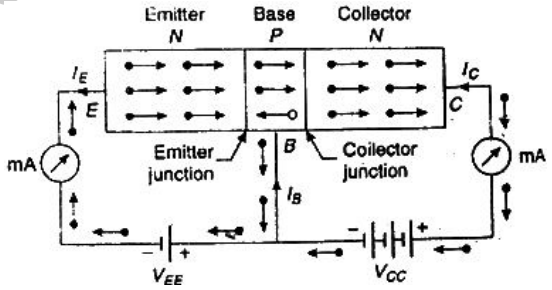
$\therefore \quad I_E = I_B + I_C$

### 2.1.2 N-P-N Transistor

**Q3. Explain three operation of NPN transistor.**

*Ans :* **(Imp.)**

The biasing of a NPN transistor is shown in fig. The emitter junction is forward biased because electrons are repelled from the negative emitter battery terminal $V_{EE}$ towards the junction. The collector junction is reverse biased because electrons are flowing away from the collector junction towards the positive collector battery terminal $V_{CC}$.




**Figure**

The operation of PNP transistor is as follows. The electron in the emitter region are repelled from the negative terminal of battery towards the emitter junction. Since the potential barrier at the junction is reduced due to forward bias and base region is very thin and lightly doped, electrons cross the P-type base region. A few electrons combine with the holes in P region and are lost as charge carriers. Now the electrons in N region (collector region) readily swept up by the positive collector voltage $V_{CC}$.

For every electron flowing out the collector and entering the positive terminal of battery $V_{CC}$. An electron from the negative emitter battery terminal enters the emitter region. In this way electron conduction takes place continuously so long as the two junctions are properly biased.

So, the current conduction in NPN transistor is carried out by electrons.

## 2.2 CURRENT COMPONENT IN TRANSISTORS

**Q4. What are the current components in transistors ?**

*Ans :* **(Imp.)**

The various current components which flow across the forward biased emitter junction and reverse - biased collector junction in PNP transistor :

The emitter current consists of the following two points :

(i) Hole current $I_{PE}$ constituted by holes (holes crossing from emitter into base).

(ii) Electron current $I_{nF}$ constituted by electrons (electrons crossing from base into the emitter)

$\therefore$ Total emitter current $I_E = I_{PE} + I_{nE}$ ... (1)

majority minority

In commercial transistors the doping of emitter region is made much heavier than base and hence the electrons current component $I_{nE}$ is negligibly small in comparison with the hole current $I_{PE}$ is negligibly small in comparison with the hole current $I_{PE}$. These in a commercial PNP transistor, the emitter current consists almost entirely of holes.

A few of holes crossing the junction $J_E$ combine with the electrons in N type base and rest of them cross the collector junction $J_C$. This reduces the number of holes which ultimately reach the collector. To reduce the number of holes so lost through recombination with electrons in N-region, the width of the base region is kept extremely small. Let $I_{PC}$ be the hole current at junction $J_C$. The different $(I_{PE} - I_{PC})$ is the recombination current $I_B$ which leaves the base as shown in figure.

In fact, electrons enter the base region through the base lead to replenish those electrons which have been lost by recombination with the holes injection into the base across $J_E$. The holes on reaching the collector junction cross this junction readily and enter the P-region of the collector.

If the emitter were open - circuited, then $I_E = 0$ i.e., $I_{PC}$ would be zero. Under this condition, the base and collector together act as a reversed diode and the collector current $I_C$ equals the reverse saturation current $I_{CO}$. Which consists of the following two parts :

$I_{nco}$ caused by electrons movin across $J_C$ from P-region to N-region.

$I_{PCO}$ caused by holes moving across $J_C$ from N-region to P-region ... (2)

$I_{CO} = I_{nco} + I_{PCO}$

In general $I_C = I_{PC} + I_{CO}$ ... (3)

majority minority

Thus, for a PNP transistor $I_E = I_B + I_C$ ... (4)

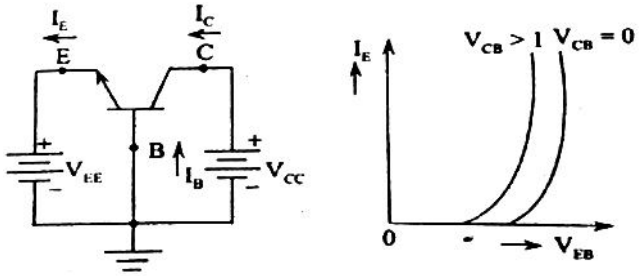
### 2.2.1 CB Configuration

**Q5. Draw the circuit diagram of CB configuration of transistor and explain its Input and Output characteristics.**

*Ans :*

In CB configuration input is applied between emitter and base and the output is taken between the collector and base terminals. Variable power supplies $V_{EE}$ and $V_{CC}$ are used respectively to forward bias emitter base junction and to reverse bias collector - base junction. The ammeters and voltmeters connected

in the input and output circuits are used to measure currents and voltages in the circuit fig shows a PNP transistor in CB configuration.




**Figure**

### Input Characteristics

The input parameters in CB configuration are input current $I_E$ and input voltage $V_{EB}$. Input characteristics are studied at a constant output voltage $V_{CB}$. A plot between various $V_{EB}$ values and corresponding $I_E$ values for a given output voltage $V_{CB}$ is called input characteristics. For each $V_{CB}$ values, $V_{EB}$ is changed in small steps and corresponding values of $I_E$ are noted.

The main features of input characteristics are :

(i) For the values of $V_{EB}$ less than certain voltage known as offset, cutoff or threshold voltage there will be very small emitter current $I_E$ flows through the circuit.

(ii) Beyond cutoff, for small values of $V_{BE}$ input current $I_E$ increases rapidly.

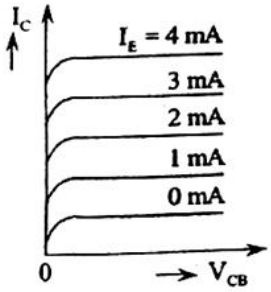
(iii) From the slope of the curves it is clear that the input resistance is low.

(iv) The input characteristic curves are similar to a forward biased diode characteristics.

(v) As output voltage $V_{CB}$ increased, the curves becomes more step.

### Output Characteristics

Output parameters in CB configuration are output voltage $V_{CB}$ and output current $I_C$. To study the output characteristics, input current $I_E$ is kept constant and $V_{CB}$ is changed in steps and the corresponding output current $I_C$ is measured, the curves are drawn from various input current $I_E$ values. The output characteristics of CB configuration are shown in fig. the output characteristics curves have three regions namely saturation region, active region and cut - off region.




### Output Characteristics of CB Configuration

#### (i) Saturation region

In this region both emitter and collector junctions are in the forward bias. As collector - base junction is in forward bias, for any small change in $V_{CB}$ a large change in $I_E$ is produced. There is a small current $I_C$ even in the absence of $V_{CB}$.

**(ii) Active region**

In this region $I_C$ remains constant for given $I_E$ even when $V_{CB}$ is changed due to this reason the transistor is operated in this region. In this region the amplification factor is slightly less than unity as some of the charge carriers emitted by the emitter are lost in the base region due to recombination. When the value of $V_{CB}$ attains a threshold or maximum value the collector current $I_C$ increases very rapidly due to avalanche effect. This effect is shown on the curves with dotted lines in the fig. In this configuration emitter junction is in forward bias and collector junction is in reverse bias.

**(iii) Cut off region**

In this region both emitter and collector junctions are in reverse bias. A small $I_C$ flows in this region even when $I_E$ is zero. This is known as leakage current $I_{CRO}$.

### 2.2.2 CE Configuration

**Q6. Explain the input and output characteristics of CE configuration of transistor with neat diagram?**

*Ans :*

**Input and output characteristics :**

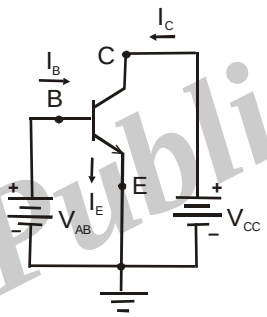





Fig. shows CE configuration circuit and its input characteristics. In this configuration in put voltage is applied between base and emitter. The output is taken at collector emitter circuit as shown in the fig. Using $V_{BB}$ and $V_{CC}$ variable power supplies, base-emitter junction is provided forward bias and collector-emitter junction in to reverse bias respectively. Input and output currents and voltages are measured using ammeters and voltmeter, connected as shown in the circuit.

**Input Characteristics**

By keeping output voltage $V_{CE}$ at a constant value, the input voltage $V_{BE}$ are noted to study the input characteristics. For various constant values of $V_{CE}$ input curves are plotted between $V_{BE}$ and $I_E$. These curves are shown in fig. The important features of input characteristic curves are:

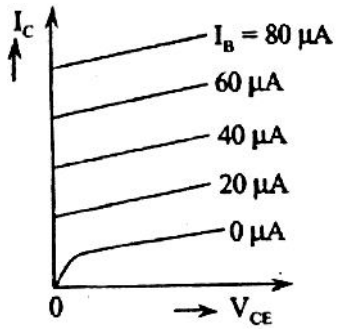
(i) These curves are similar to forward biased diode.

(ii) The slope of the curves is less than that of CB input characteristic curves. So input resistance in CE configuration is small.

**Output Characteristics**

The output characteristics are drawn between the output voltage $V_{CE}$ and output current $I_E$ for a constant input current $I_B$ values are drawn between $V_{CE}$ and $I_C$.

The output characteristics are studied by dividing into three regions namely saturation, active and cut off regions as shown in fig.




**(i) Saturation Region**

In this region both emitter and collector junctions are in forward biased condition. This region corresponds to low values of $V_{CE}$ the changes in $I_C$ are not according to changes in $I_E$ in this region.

**(ii) Active Region**

In this region of operation, base emitter junction is in forward bias and collector - emitter junction is in reverse bias.

At now values of $I_B$ the effect odf $V_{CE}$ on $I_C$ is very small. But at higher values of $I_B$, there is large change in the values of $I_C$ with the voltage $V_{CE}$, as $I_B$ values are small compared with $I_C$ values, the current amplification factor ($\beta$) will be very large. Hence in this region of CE configuration transistor is used as an amplifier. The signal get distorted if its value goes beyond the active region. So transistor works as an ideal amplifier in this region only.

**(iii) Cut-off Region**

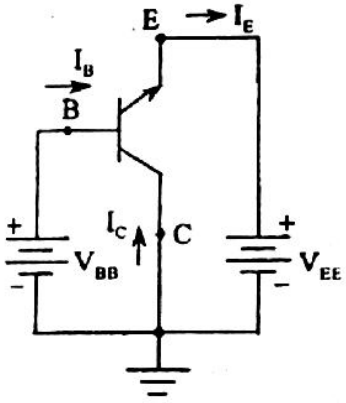
In this region both the emitter and collector junctions are in reverse biased condition. Collector current $I_C$ exists even if $I_B$ is zero in this region. This current is due to minority charge carriers which are crossing the reverse biased collector-emitter junction and is designated as $I_{CEO}$.

### 2.2.3 CC Configuration

**Q7. Explain the input and output characteristics of common collector configuration?**

*Ans :*

CC configuration of a transistor is shown in fig. The input is applied at base collector junction while the output is taken between emitter and collector.



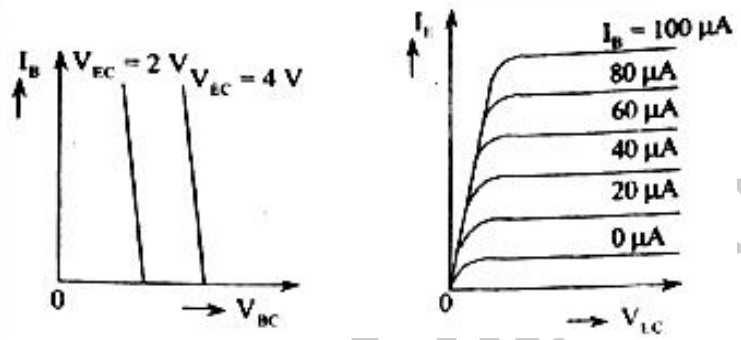
The only main difference between CE configuration CC configuration is placing of a load resistance. The load resistance is connected in this configuration in emitter circuit whereas in CE configuration it is connected in collector circuit. Therefore the operation of both the circuit are almost similar.

**Input Characteristics**

Input characteristics curves in CC configuration are plotted between $V_{CB}$ and $I_B$ at various constant values of $V_{CE}$ from fig.

We have $V_{CE} = V_{CB} + V_{BE}$ or $V_{BE} = V_{CE} - V_{CB}$

We know that under forward bias the voltage across silicon and germanium are 0.7 v and 0.3 v respectively. From equation $I_E = I_B + I_C$ if $V_{CB}$ and $V_{CE}$ are equal then $V_{BE}$ becomes zero due to this reason for small change in $V_{CB}$ the current $I_B$ rapidly falls to zero.




Since, $I_C = I_E$ the output characteristics of CE and CC configuration are same.

## 2.3 RC COUPLED AMPLIFIER

**Q8. Describe the construction and working of RC - coupled Amplifier.**

*Ans :* **(Imp.)**

Figure shows a two stage R-C coupled amplifier using common -emitter configuration. The two transistors are identical and a common power supply $V_{CC}$ is used. The resistors $R_1$, $R_2$ and $R_e$ form the biasing and stabilization network. The emitter bypass capacitor $C_e$ offers low reactance path to signal. The resistor $R_L$ is used as a load impedance, the input capacitor couples a.c. signal voltage to the base of transistor. In the absence of , the signal source will be in parallel with $R_2$ and the bias voltage of the base will be changed, thus, the function of $C_{in}$ is to allow only the alternating current from signal source to flow into input circuit.

The output of the first stage is coupled to the input of second stage through coupling capacitor C. This allows the a.c. component of the signal to pass to the second stage and blocks the d.c component. As the coupling from one stage to the next stage is achieved via coupling capacitor followed by a connection to shunt resistor, therefore, the amplifier is known as resistance capacitance coupled amplifier.

When a.c. signal is applied to the base of the first transistor, it appears across collector load $R_L$ in the amplified form. Through coupling capacitor C, the amplified signal is transferred to the next stage of the amplifier. This is further amplified by the next stage. So the cascaded stages amplify the signal and thus the overall gain is considerably increased. The phase of output is the same as that of input because the phase is reversed twice by two transistors as they are in common emitter configuration.

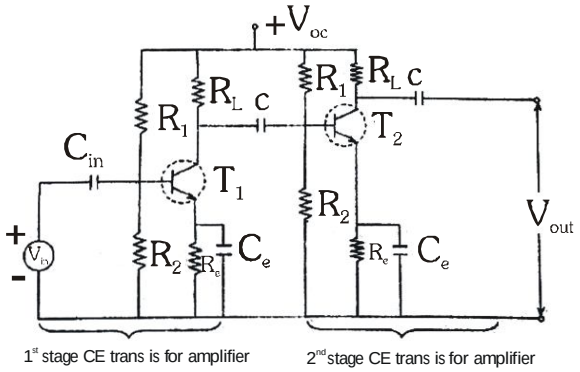



**Fig. : Two Stage RC Coupled Amplifier**

## 2.4 Feedback, General Theory of Feedback

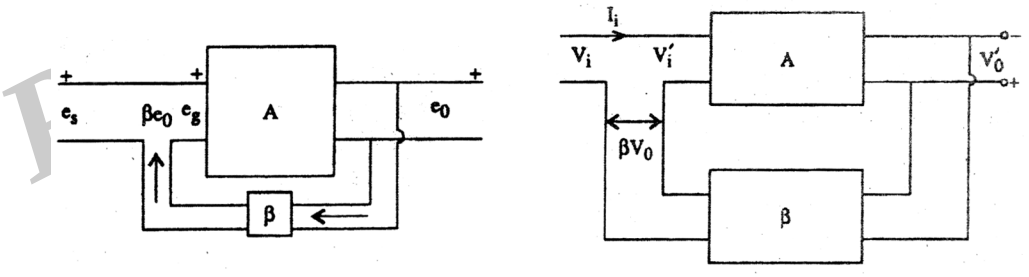
**Q9. Give the general theory of feed back.**

**(OR)**

**Explain the barkhausen criterion for oscillations.**

*Ans :* **(Imp.)**

The general theory of feedback can be understood with the help of block diagram shown in fig. The feedback amplifier has two parts, i.e. amplifier and feed back circuit. The feed back circuit usually consists of resistors. This returns a fraction (say) ($\beta$) of the output voltage back to the input. Let A be the gain of the amplifier, i.e. the ratio of output voltage $V_0$ to the input voltage $V_i$ this is the gain of the amplifier without feed back. The feed back network extracts a voltage $V_f = \beta V_0$ from the output $V_0$ of the amplifier.




This voltage is added (positive feed back) or subtrcted (negative feed back) from the signal voltage $V_s$. Now

$$V_i = V_s + V_f = V_s + \beta V_o$$

$$V_i = V_s - V_f = V_s - \beta V_o$$

The quantity $\beta = V_f / V_o$ is called ratio or feedback fraction. Let $\Delta_f$ be the overall gain (gain with feedback) of the amplifier. This is defined as the ratio of out put voltage $V_0$ to the applied signal voltage $V_s$.

Thus, gain without feedback.

$$A = \frac{V_0}{V_1}$$

(or) $V_0 = Av_i$ ... (1)

Further $V_i = V_s + \beta V_o$ ... (2)

From equation (1) and (2), we get

$$V_0 = A[V_s + \beta V_o] = AV_s + A\beta V_0$$

(or) $V_0 [1 - A\beta] = AV_s$

$$\therefore \quad \frac{V_0}{V_s} = \frac{A}{1 - A\beta} \quad \text{... (3)}$$

But the resultant gain of the amplifier with feed back.

$$A_f = \frac{\text{Output voltage}}{\text{Input signal voltage}} = \frac{V_o}{V_\beta} \quad \text{... (4)}$$

From equation (3) and (4)

$$A_f = \frac{A}{1 - A\beta} \text{ positive feed back}$$

$$A_f = \frac{A}{1 + A_\beta} \text{ negative feed back}$$

Now we consider the following three cases;

(i) When $|1 + A\beta| > 1$, $|A_f| < |A|$, feedback is negative

(ii) When $|1 + A_\beta| < 1$, $|A_f| > |A|$, feedback is positive

(iii) Considering the case of positive feed, if $A\beta = 1$, $A_f = \infty$ this is possible only when input is zero.

Thus, the amplifier is then capable of producing output even when input is zero. Under this situation, amplifier works as an oscillator.

The condition $A_\beta = 1$ is called as Brakhausen condition for oscillators.

## 2.5 Concept of Oscillators

**Q10. Explain how a transistor acts as an oscillator.**

*Ans :*

We have seen that an amplifier is an energy converter. This takes energy from supply source and converts. Into a.c. signal at signal frequency. In the absence of Input signal, there is no energy conversion. On the other hand, oscillator does not require an external input source. This produces an output signal without signal so long as d.c. power source is connected.

Hence, the oscillator may be defined as a circuit which generates an a.c. output signal without any externally applied input signal or a circuit which converts d.c. energy into a.c. energy at very high frequencies. Oscillators may be broadly divided into following two groups:

## 1. Sinusoidal Oscillators

These oscillators produce sine waveform, i.e. f sinu soidal oscillators.

The following are the examples of sinusoidal oscillators:

(i) Tuned collector, oscillator

(ii) Hartely oscillator

(iii) Colpitt's oscillator

(iv) Negative resistance oscillator

(v) Phase shift oscillator

(vi) Crystal oscillator

## 2. Non-sinusoidal Oscillators

These oscillators produce square, rectangular, sawtooth, wave forms, multi vibrators.

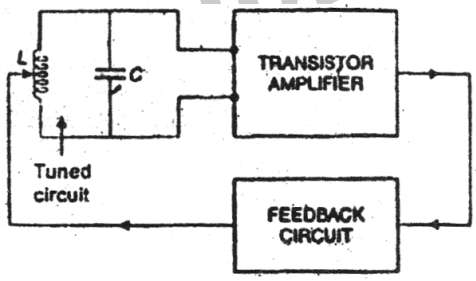
The essentials of a transistor oscillator are shown in fig.

Essentials of transistor oscillator this consists of

(i) tank circuit

(ii) amplifier and

(iii) feed back circuit.






### (i) Tank Circuit

The tank circuit consists of an oscillator circuit, i.e. an inductance coil L connected in parallel with capacitor C. the frequency of oscillations depend upon the values of inductance and capacitance.

### (ii) Amplifier

The amplifier receives d.c. power from the battery and converts it into a.c. power. The oscillations of tank circuit are applied to the input of amplifier, the amplifier increases the strength of oscillations. The output of the transistor is supplied to the tank circuit to compensable the losses of tank circuit.

### (iii) Feed back circuit

This circuit supplies a part of the collector energy to the tank circuit. The transistor produces a phase change of 180° and feed back circuit also produces phase change of 180° So there is a positive feedback thus oscillations take place.

## 2.6 Phase Shift Oscillator (or) Expression for Frequency of Oscillator

**Q11. Describe the working of phase shift oscillator.**

*Ans :* **(Imp.)**

We have mentioned that a tank circuit (L-C circuit) is the essential part of the oscillator circuit. But this is not always an essential requirement. The essential requirement is feed back from the output circuit to the input circuit in proper phase. This is necessary to overcome the circuit losses and maintain oscillations in oscillator circuit.

We know that a resistance - capacitance (R-C) combination provides a current which leads the applied voltage by certain angle. With a proper choice of R and C, a phase shift of 60° per section may be achieved. In phase shift of 180° is obtained with three cascade sections of R-C combination.

**Circuit Arrangement**

The Circuit arrangement of a phase shift oscillator using NPN transistor in common emitter configuration is show in fig.

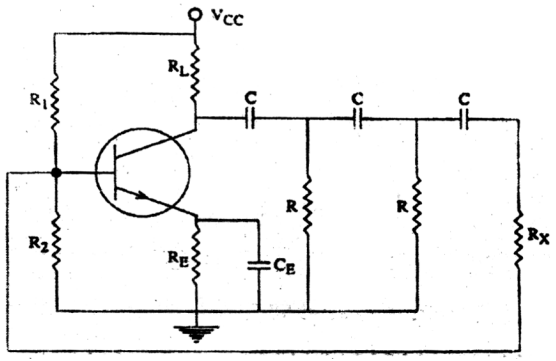
In this circuit $R_1 - R_2$ combination provides the proper d.c. base biasing R, is the load which controls the collector voltage. $R_e - C_e$ combination provides the temperature stability of operating point. The output of the amplifier goes to a feedback network which consists of three identical R – C sections. It should be noted that the last section contains a resistance $R^1 = R - h_{ie}$ because this resistance $R^1$ is connected to the base of transistor which has input resistance h. since the resistor $R^1$ is connected with the base of transistor, the input resistance $h_{ie}$ of the transistor is added to it give a total resistance R.

**Circuit Action:**

Here R - C network produces a phase shift of 180° between input and output voltages. Since common emitter amplifier produces a phase shift of 180°, the total phase change becomes 360°, which is the essentiald requirement of sustained oscillators the R - C phased shift networks serve as frequency determining circuit. These oscillators are used for audio frequency ranges.

The frequency of oscillations of the given phase - shift oscillator is given by

$$f = \frac{1}{2\pi\sqrt{10}RC}$$



# Short Question and Answers

**1. What is meant by transistor biasing, (or) Different types of transistors?**

*Ans :*

The transistor biasing is shown in fig. The emitter - base junction is always forward - biased while the collector base junction is always reversed biased. For this purpose a battery $V_{EE}$ is connected between emitter and base while a battery $V_{CC}$ is connected between collector and base. In fig (a), the emitter - base junction of P-N. P transistor is forward - biased by connecting the positive terminal of $V_{PN}$ to emitter and negative terminal to base.

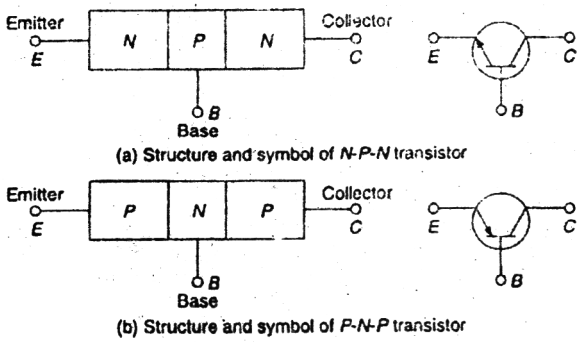



**Fig. : N-P.N and P.N-P Transistor**

(a) PNP Transistor biasing (b) NPN transistor baising

Similarly, in fig (b), the emitter - base junction of N-P-N transistor is foward. biased by connecting the negative terminal of $V_{EE}$ to emitter and positive terminal to base. In fig(a), the collector base junction of a P-N-P transistor is reverse, biased by connecting the negative terminal of $V_{CC}$ to collector while positive terminal to base similarly, in fig, the collector - base junction of N-P-N transistor is reverse biased by connecting the positive terminal of $V_{CC}$ to collector while negative terminal to base.

We have seen that forward - biased emitter - base junction has a low resistance path where a reverse - biased collector - base junction has a low resistance path where a reverse - biased collector - base junction has high resistance path.

**2. What are transistor configurations?**

*Ans :*

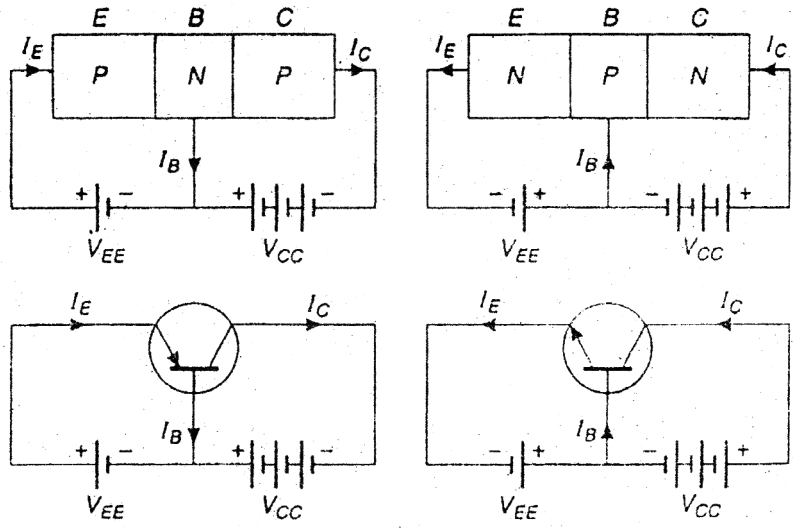
Following are the three types of transistor circuit Configurations:

1. Common - base (CB)
2. Common - emitter (CE)
3. Common - collector (CC)

Here the term 'Common' is used to denote the transistor lead which is common to the input and output circuits. This is because when a transistor is connected in a circuit for terminals are required

(two for input and two for output) while a transistor has only three terminals. The difficulty is removed by making one terminal of the transistor 'common' to both input and output terminals. The common terminal is generally grounded. Each configuraiton has specific advantages and disadvantages, it should be remembered that regardless the circuit configuration. The emitter is always forward - based while the collector is always reverse - biased.

The different configurations of a PNP transistor are shown in fig.




**(a) P-N-P transistor biasing (b) N-P-N transistor biasing**

In common base configuration, the base is common to both input and output and is earthened. The input is given across emitter and base while the output is taken across collector and base.

In common emitter configuration the emitter is common to both input and output and is earthed. The input is given across base and emitter while the output is taken across collector collector and emitter.

In common collector configuration, the collector is common to both input and output and is earthed. The input is given across base and collector while the output is taken across emitter and collector.

### 3. Define current Amplification factor.

*Ans :*

When no signal is applied, then the ratio of the collector current to the emitter current is called d.c. alpha ($\alpha_{dc}$) of a transistor.

$$(\alpha_{dc}) = \frac{-I_C}{I_E}$$

(Negative sign signifies that $I_E$ flows into transistor while $I_C$ flows out of it). If we write $\alpha_{dc}$ simply by $\alpha$, then

$$\alpha = \frac{-I_C}{I_E} \quad \text{... (1)}$$

a of a transistor is a measure of the quality of a transistor. Higher is the value of $\alpha$, better is the transistor in the sense that collector current approaches the emitter current.

From equation (1), considering only magnitudes of the currents

$I_C = \alpha \cdot I_E$

and hence $I_B = I_E - I_C$

$\therefore \quad I_B = I_E - \alpha I_E = I_E (1 - \alpha)$ ... (2)

When signal is applied, the ratio of change in collector current to the change in emitter current at constnat collector base voltage is defined as current amplification factor.

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \quad \text{... (3)}$$

For all physical purpose, $\alpha_{dc} = a_{ac} = a$ and practical values in commercial transistors range from 0.9 to 0.99

Total collector current consists of the following two parts:

(i) The current produced by normal transistor action, ie. component controlled by emitter current. This is due to the majority carrier and its value is $\alpha I_E$.

(ii) The leakage current $I_{leakage}$. This current is due to the motion of minority carrier across base - collector junction on account of it being reverse - biased. This is much smaller than $\alpha I_E$. The leakage current is abbreviated as $I_{CBO}$' i.e. collector base current with emitter open.

$\therefore$ Total collector current

$I_C = \alpha I_E + I_{CBO}$

majority minority

**4. What is meant by base current amplification factor?**

*Ans :*

**Base Current Amplification Factor ($\beta$)**

When no signal is applied, then the raito of collector curret to the base current called dc beta ($\beta_{dc}$) of transistor.

$$(\beta_{dc}) = \beta = \frac{I_C}{I_B}$$

When signal is applied, the ratio of change in collector current to the change in base current amplification factor thus,

$$(\beta_{dc}) = \beta = \frac{\Delta I_C}{\Delta I_B}$$

Form equation (5) $I_C - \beta I_B$

Almost in all transistor, the base current is less than 5% of the emitter current. Due to this fact, $\beta$ is generally greater than 20. Usually, $\beta$ ranges from 20 to 500. Hence, this configuration is frequently used when appreciable current gain as well as voltage gain is required.

Total collector current $I_C = \beta I_B + I_{CEO}$ where $I_{CEO}$ is the leakage current. It is called $I_{CEO}$, the subscript CEO stands for collector to emitter with base open.

**5. Derive the relation between $\alpha$ & $\beta$ ?**

*Ans :*

**Relation between $\alpha$ and $\beta$**

We know that

$$\alpha = \frac{I_C}{I_E} \text{ and } \beta = \frac{I_C}{I_B}$$

$$I_E = I_B + I_C \text{ or } I_B = I_E - I_C$$

Now

$$\beta = \frac{I_C}{I_E - I_C} = \frac{I_C / I_E}{1-(I_C / I_E)} = \frac{\alpha}{1-\alpha} \quad \text{... (1)}$$

Cross - multiplying equation (1) we get

$$\beta = (1 - \alpha) = \alpha \text{ or } \beta - \beta\alpha = \alpha \text{ or } \beta = \alpha(1 + \alpha)$$

$$\therefore \quad \alpha = \frac{\beta}{1+\beta} \quad \text{... (2)}$$

It can be seen that $1 - \alpha = \frac{\beta}{1+\beta}$ ... (3)

**6. What is meant by current amplification factor?**

*Ans :*

Current amplification factor ($\gamma$): when no signal is applied, the ratio of emitter current to the base current is called as d.c. gamma ($\gamma_{dc}$) of the transistor.

$$(\gamma_{dc}) = \gamma = \frac{I_E}{I_B} \quad \text{... (1)}$$

When signal is applied, then the ratio of chane in emitter current to the change in base current is known as current amplification factor $\gamma$

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \quad \text{... (2)}$$

This configuration provides about the same current gain as common emitter circuit as $\Delta I_E \approx I_C$ but the voltage gain is always less than one.

**7. How does transistor work as an amplifier?**

*Ans :*

The weak signal to be amplified is applied between emitter - base circuit and the output is taken a cross the load resistor $R_L$ connected in the collector circuit. A d.c. voltage $V_{EE}$ is also connected in the input circuit.

A small change in signal voltage produces, an appreciable. Change in emitter current because the input circuit has low resistance. Now due to the transistor action, the change in emitter current almost causes almost the same change in collector current. When the collector current flows through the load. Resistance $R_L$ a large voltage is developed across it. In this way, a weak signal applied in the input circuit appears in the amplified form across the output circuit.

Let a small voltage change $\Delta V_1$ between emitter and base causes a relatively large emitter - current change $\Delta V_E$ we define by the symbol a that fraction of this current change which is collected and passes through $R_L$ thus,

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

i.e., $\Delta I_C = \alpha \Delta I_E$

The change in output voltage across the load resistor

$$\Delta V_o = R_L \times \Delta I_C$$
$$= R_L \times \alpha.dI_E$$

Under these circumstances, the voltage amplification

$$A = \frac{\Delta V_o}{\Delta V_i}$$

Will be greater than unity and the transistor acts as an amplifier. If the dynamic resistance of the e junction be $r_e$. Then $\Delta V_i = r_e, \Delta I_E$

$$A = \frac{R_L \times \alpha.\Delta I_E}{r_e.\Delta I_E} = \frac{\alpha R_L}{r_e}$$

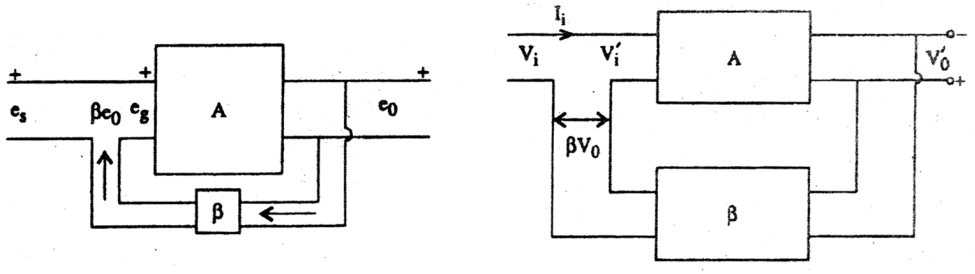
**8. Give the general theory of feed back.**

**(OR)**

**Explain the barkhausen criterion for oscillations.**

*Ans :*

The general theory of feedback can be understood with the help of block diagram shown in fig. The feedback amplifier has two parts, i.e. amplifier and feed back circuit. The feed back circuit usually consists of resistors. This returns a fraction (say) ($\beta$) of the output voltage back to the input. Let A be the gain of the amplifier, i.e. the ratio of output voltage $V_0$ to the input voltage $V_i$ this is the gain of the amplifier without feed back. The feed back network extracts a voltage $V_f = \beta V_0$ from the output $V_0$ of the amplifier.



This voltage is added (positive feed back) or subtrcted (negative feed back) from the signal voltage $V_s$. Now

$$V_i = V_s + V_f = V_s + \beta V_o$$

$$V_i = V_s - V_f = V_s - \beta V_o$$

The quantity $\beta = V_f / V_o$ is called ratio or feedback fraction. Let $\Delta_f$ be the overall gain (gain with feedback) of the amplifier. This is defined as the ratio of out put voltage $V_0$ to the applied signal voltage $V_s$.

Thus, gain without feedback.

$$A = \frac{V_0}{V_1}$$

(or) $V_0 = Av_i$ ... (1)

Further $V_i = V_s + \beta V_o$ ... (2)

From equation (1) and (2), we get

$$V_0 = A[V_s + \beta V_o] = AV_s + A\beta V_0$$

(or) $V_0 [1 - A\beta] = AV_s$

$$\therefore \quad \frac{V_0}{V_s} = \frac{A}{1 - A\beta} \quad \text{... (3)}$$

But the resultant gain of the amplifier with feed back.

$$A_f = \frac{\text{Output voltage}}{\text{Input signal voltage}} = \frac{V_o}{V_\beta} \quad \text{... (4)}$$

From equation (3) and (4)

$$A_f = \frac{A}{1 - A\beta} \text{ positive feed back}$$

$$A_f = \frac{A}{1 + A_\beta} \text{ negative feed back}$$

Now we consider the following three cases;

(i) When $|1 + A\beta| > 1$, $|A_f| < |A|$, feedback is negative

(ii) When $|1 + A_\beta| < 1$, $|A_f| > |A|$, feedback is positive

(iii) Considering the case of positive feed, if $A\beta = 1$, $A_f = \infty$ this is possible only when input is zero.

Thus, the amplifier is then capable of producing output even when input is zero. Under this situation, amplifier works as an oscillator.

The condition $A_\beta = 1$ is called as Brakhausen condition for oscillators.

**9. Explain how a transistor acts as an oscillator.**

*Ans :*

We have seen that an amplifier is an energy converter. This takes energy from supply source and converts. Into a.c. signal at signal frequency. In the absence of Input signal, there is no energy conversion. On the other hand, oscillator does not require an external input source. This produces an output signal without signal so long as d.c. power source is connected.

Hence, the oscillator may be defined as a circuit which generates an a.c. output signal without any externally applied input signal or a circuit which converts d.c. energy into a.c. energy at very high frequencies. Oscillators may be broadly divided into following two groups:

**1. Sinusoidal Oscillators**

These oscillators produce sine waveform, i.e. f sinu soidal oscillators.

The following are the examples of sinusoidal oscillators:

(i) Tuned collector, oscillator

(ii) Hartely oscillator

(iii) Colpitt's oscillator

(iv) Negative resistance oscillator

(v) Phase shift oscillator

(vi) Crystal oscillator

**2. Non-sinusoidal Oscillators**

These oscillators produce square, rectangular, sawtooth, wave forms, multi vibrators.

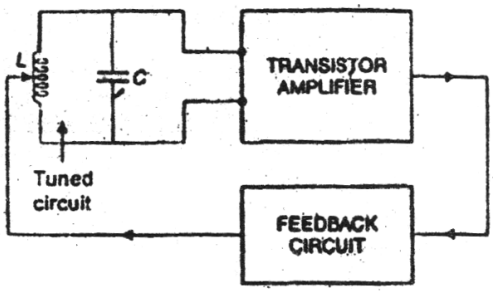
The essentials of a transistor oscillator are shown in fig.

Essentials of transistor oscillator this consists of

(i) tank circuit

(ii) amplifier and

(iii) feed back circuit.



### (i) Tank Circuit

The tank circuit consists of an oscillator circuit, i.e. an inductance coil L connected in parallel with capacitor C. the frequency of oscillations depend upon the values of inductance and capacitance.

### (ii) Amplifier

The amplifier receives d.c. power from the battery and converts it into a.c. power. The oscillations of tank circuit are applied to the input of amplifier, the amplifier increases the strength of oscillations. The output of the transistor is supplied to the tank circuit to compensable the losses of tank circuit.

### (iii) Feed back circuit

This circuit supplies a part of the collector energy to the tank circuit. The transistor produces a phase change of 180° and feed back circuit also produces phase change of 180° So there is a positive feedback thus oscillations take place.

# Problems

**1. Calculate the gain of a negative feedback amplifier with internal gain = 200 and feed back factor $\beta$ = 1/20.**

*Sol :*

$$A_i = \frac{A}{1+A\beta} = \frac{200}{1+200\times(1/20)} = \frac{200}{1+20} = \frac{200}{21} = 9.5$$

**2. The overall gain of a multistage amplifier is 100. When negative feedback is applied the gain reduces to 10. Find the fraction of the output that feedback to the input.**

*Sol :*

We know that

$$A_i = \frac{A}{1+A\beta}$$

Here,

$A_i = 10$ and $A = 100$

$$10 = \frac{100}{1+100\beta} \text{ or } 10 + 100\,\beta - 100$$

$$\beta = \frac{100-10}{1000} = \frac{90}{1000} = \frac{9}{100} = 0.09$$

**3. Calculate the gain of (i) a positive feedback amplifier and (ii) a negative feedback amplifier with an internal of A = 100 and feedback factor $\beta$ = 1/100.**

*Sol :*

(i) For positive feedback,

$$A_i = \frac{A}{1-A\beta}$$

$$= \frac{100}{1-100\times\left(\frac{1}{1000}\right)} = \frac{100}{1-0.1} = \frac{100}{0.9} = 111.1$$

(ii) For negative feedback $\qquad \frac{100}{1+0.1}$

$$A_f = \frac{A}{1-A\beta}$$

$$A_f = \frac{100}{1+100\times\left(\frac{1}{1000}\right)} = \frac{100}{1+0.1} = \frac{100}{1.1} = 90.909 = 90.91$$

**4. With a negative feedback, an amplifier gives an output of 10V with an input of 0.5V. When the feedback is removes, it required 0.25V input for the same output. Calculate** (i) gain without feedback and (ii) feedback fraction **β.**

*Sol :*

(i) Gain without feedback

$A = 10 / (0.25) = 40$

(ii) Gain with feedback

$A_f = 10 / (0.5) = 20$

Now

$$A_f = \frac{A}{1+\beta A} \text{ or } 20 = \frac{40}{1+40\beta}$$

$20 (1 + 40 - \beta) = 40$ or $(20 + 800\beta) = 40$

$800\beta = 40 - 20 = 20$

$$\beta = \frac{20}{800} = \frac{1}{40}$$

---

**5. The gain of an amplifier is 4000. If the feedback factor is 0.04, which is the closed loop gain of the amplifier. How the loop gain changes when the gain is increased to 8000.**

*Sol :*

Given that

$A = 4000, \ \beta = 0.04$

Closed loop gain,

$$A_f = \frac{A}{1+\beta A}$$

$$\therefore \quad Af_f = \frac{4000}{1+4000\times 0.04} = 24.84$$

When

$A = 8000$

$$A_f = \frac{8000}{1+8000\times 0.04} = 24.92$$

These two values of $A_f$ are almost equal. Hence the changes in $A_f$ are very small when "A" has large values. Observe that $A_f = \frac{1}{\beta} = \frac{1}{0.04} = 25$.

**6. The gain of an amplifier is 40. When feedback is applied gain has decreased to 10. Find the percentage of feedback.**

*Sol :*

Given that

$$A = 40 \text{ and } A_f = 10 \quad A_f = \frac{A}{1 + A\beta}$$

$$10 = \frac{40}{1 + 40\beta}$$

$$\beta = \frac{3}{40}$$

Percentage of feedback $= \frac{3}{40} \times 100 = 7.5\%$

# Choose the Correct Answers

1. The majority charge carries are supplied from region of transistor. [ c ]

   (a) Collector (b) Base

   (c) Emitter (d) None

2. The collector - base junction is biased [ b ]

   (a) Forward (b) Reversed

   (c) Both (d) Alternately

3. As a standard convertion, a current entering into the transistor is taken as [ a ]

   (a) Positive (b) Negative

   (c) Both (d) None

4. Base - current amplificatiion factor $\beta$ in CE configuration is given by [ b ]

   (a) $\frac{I_B}{I_C}$ (b) $\frac{I_C}{I_B}$

   (c) $\frac{I_E}{I_B}$ (d) $\frac{I_E}{I_C}$

5. The gain of the feed back amplifier with negative feed back is given by [ d ]

   (a) $A_f = \frac{A}{A + A\beta}$ (b) $A_f = \frac{I}{A + \beta}$

   (c) $A_f = \frac{\beta}{A + \beta}$ (d) $A_f = \frac{A}{1 + A\beta}$

6. The frequency osicillations of the given phase - shift oscillator is given by [ b ]

   (a) $f = \frac{1}{2\pi RC}$ (b) $f = \frac{1}{2\pi\sqrt{1DRC}}$

   (c) $f = \frac{RC}{2\pi\sqrt{1D}}$ (d) $f = \frac{1}{2\pi\sqrt{1DR}}$

7. Which among the following is a barkhausen cordition for oscillations [ a ]

   (a) $A\beta = 0$ (b) $A\beta = 1$

   (c) $A\beta = \infty$ (d) None

8. In cc configuration, the current amplification factor & is given by [ b ]

(a) $\frac{I_E}{I_B}$ (b) $\frac{I_C}{I_B}$

(c) $\frac{I_B}{I_E}$ (d) None

9. Relation between a and p is given by [ b ]

(a) $1 - \alpha = \frac{1}{1-\beta}$ (b) $1 - \alpha = \frac{1}{1+\beta}$

(c) $\propto = \frac{1}{1+\beta}$ (d) $\alpha - 1 = \frac{1}{1+\beta}$

10. Which of the following is correct expression [ c ]

(a) $v = \frac{1}{1=\alpha}$ (b) $v = 1 + \beta$

(c) a and b (d) None

# Fill in the Blanks

1. Transistors are made either from _____ or _____ crystal.
2 _____ a sandwich of one type of semiconductor material between two layers of the other type.
3. The mitter region is doped _____.
4. Current conduction is NPN transistor is carried out by _____.
5. The quantity $\beta = \frac{V_f}{V_0}$ is called _____ fraction.
6. The feedback amplifier has two parts _____ and _____ circuit.
7. The disadvantage of feedback is that it decreases the _____ of the amplifier.
8. In current feedback, the voltage feedback to the input terminals is _____ to current through the load.
9. Tank circuit, _____, _____ are essentials of transistor oscillator.
10. Each RC network in a phase shift oscillator produces _____ phase shift.

**ANSWER**

1. Silicon / Germanimum
2. Junction Transistor
3. Heavily
4. Electrons
5. Feedback
6. amplifier / feedback
7. Gain
8. Proportional
9. Amplifier, Feedback
10. 60°

UNIT III

**Special devices -** Construction and Charcteristis: Photo diode - Shockley diode - Solar cell, Opto-couplers - Field Effect Transistor (FET) - FET as an Amplifier - Uni Junction Transistor (UJT), UJT as a relaxation oscillator - Silicon controlled rectifier (SCR) - SCR as a switch.

## 3.1 Construction and Characteristics of Photo Diode

**Q1. Describe the construction and characteristics of photodiode and mention its uses.**

*Ans :* **(Imp.)**

### Photodiode

Photodiode is an opto electronic device in which light signals are converted into electrical signals by using photo emissive effect. When the light is incident on the material the electrons are ejected from the surface of the material its known as photo emissive effect.

The symbol of photodiode is as shown in figure (1).

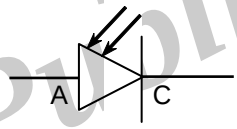



**Figure 1**

### Principle of Operation

The incident light produces electron hole pairs in the depletion regions. Then the separation of electrons and holes takes place and the photo current flows though the circuit.

### Construction

Figure(2) illustrates the cross sectional view of photodiode. A thin heavily doped p-type layer is placed on the top of lightly doped n-type layer. The depletion region is formed between p-type and n-type layer and is deeply penetrates into n-type layer. The p-type layer is exposed to the light as shown in figure (2).

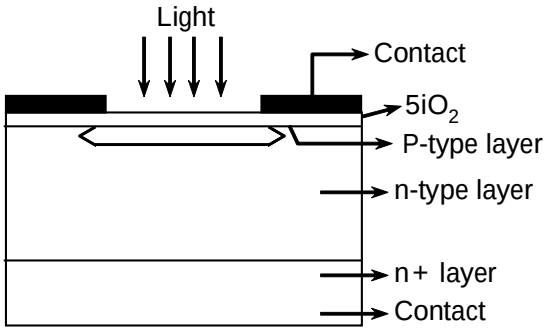



**Figure 2**

### Operation

When the light is illuminated on p-type layer, The photons from light Energy will collides with valency electrons. From this the valency electrons gets sufficient energy to separate from the parent atoms. In this manner electron hole pair are generated at PN junction; and there minority charge carriers results a reverse current flow. From this point it is clear that increasing the illumination causes increases in minority charge carriers and it results raise in reverse current flow the operation is briefly explained with he diagram as shown in figure (3).

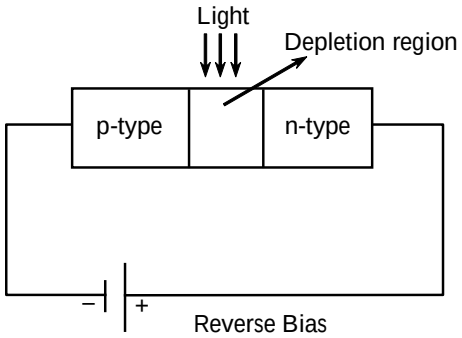



**Figure 3**

### Characteristics

Typical photodiode characteristics are as shown in figure.

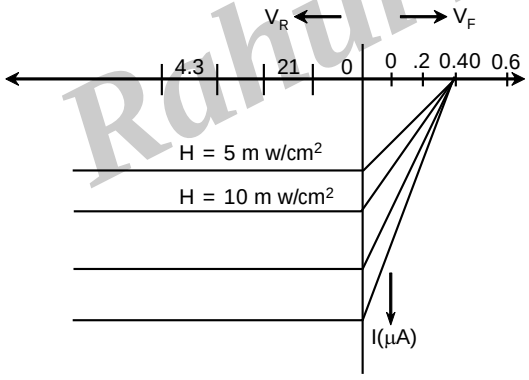



**Figure 4**

Where, there is no light is applied the current flow through the diode is zero and that current is known as dark current. The plots are observed at different illumination levels.

### Uses

The uses of photodiode include,

1. Light detectors
2. Optical detectors (or) demodulators
3. Sound track films
4. Electronic operated switches
5. Light operated switches
6. Computer punching cards and paper.
7. Encoders.

## 3.2 Shockley Diode

**Q2. What is Shockley diode ?**

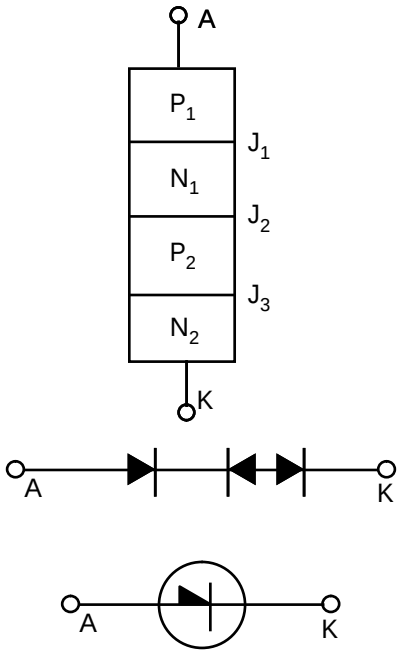
**(OR)**

**Explain working and V-I characteristics of schokley diode?**

*Ans :* **(Imp.)**

A Shockley diode is a two terminal, three junction, four-layer p-n-p-n semiconductor device. It consists of four alternate p-type and n-type semiconductor layers in a single crystal. It was invented by William Shockley. It is used primarily for switching applications. It is similar to a thyristor with detached gate.

The schematic diagram of Shockley Diode is shown in figure. It is equivalent to three junction diodes connected in series as shown in figure. The symbol of Shockley Diode is shown in figure. Here A terminal represents the anode and K terminal represents the cathode.



### Shockley Diode Working

#### (i) Under Forward biased

When this diode is forward biased (i.e., anode is positive w.r.t. Cathode), junctions J1 and J3 would be forward biased while junction J2 would be reverse biased. Hence, it offers a very high resistance to the current flow.

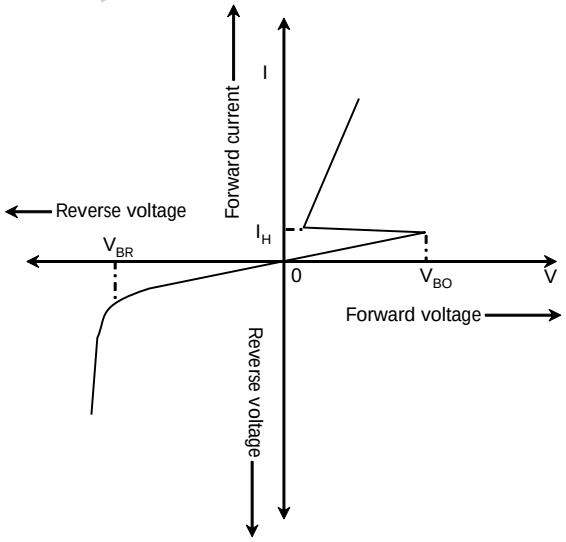
As the forward voltage increases, the reverse bias across junction J2 is also increased. At some forward voltage (called breakover voltage VBo), reverse breakdown of junction J2 occurs. Since this breakdown results in reduced resistance, this diode presents a very low resistance. Therefore it turns into conduction mode and acts as a closed switch thereby current starts flowing through it.

#### (ii) Under Reversed biased

When this diode is reversed biased (i.e., anode is negative w.r.t. cathode), junctions J1 and J3 would be reverse biased while junction J2 would be forward biased. If reverse voltage is increased sufficiently, the reverse voltage reaches the reverse breakdown voltage (VBR). At this voltage, junctions J1 and J3 would go into reverse voltage breakdown. The reverse current flowing through them would rise rapidly and the heat produced by this current flow could burn the whole device. For this reason, Shockley diode should never be operated with a reverse voltage greater than reverse voltage breakdown.

### I-V characteristics of the Shockley diode

The I-V characteristics is shown in figure.




### Shockley diode applications

1. It is used as a switch in the circuits to turn on an SCR.
2. It finds application as a relaxation oscillator.

## 3.3 Solar Cell

**Q3. Explain the working of a solar cell and draw its I-V characteristics.**

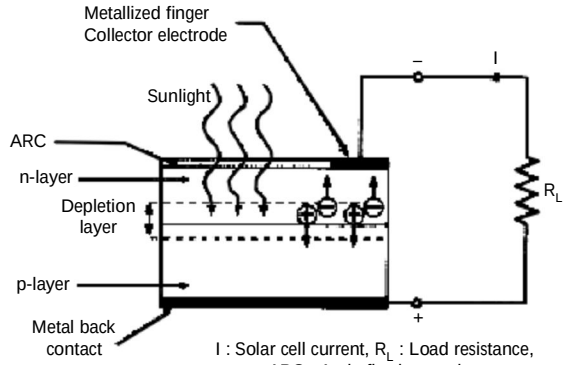
*Ans :*

Solar cell is basically a p-n junction diode which generates emf when solar radiation falls on the p-n junction. It works on the principle of photovoltaic effect.

### Construction

Solar cell consists of a p-n junction such that p-type silicon is down side and n-type silicon is upside. p-type silicon is coated with a metal act as a back contact. A metallic grid is deposited on the to of the n-type silicon which act as front contact.

Thus an emf called photovoltage is produced between these two electrodes. When a load is connected between these two electrodes a current passes through it.




I : Solar cell current, $R_L$ : Load resistance,
ARC : Antireflective coating
Sectional view of a sloar cell

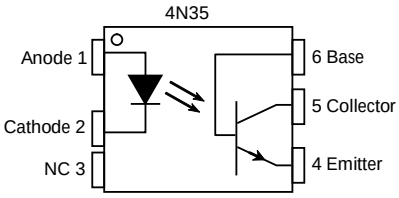
## 3.4 Opto Couplers

**Q4. What is opto coupler, explain working and applications.**

*Ans :* **(Imp.)**

The optocoupler is a circuit or component which optically couples the signal of one circuit to the other circuit. Since the circuits are coupled

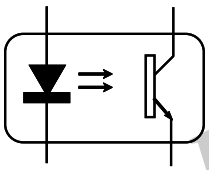
optically, it provides electrical isolation between the two circuits. The optocoupler is also known as an optoisolator or Photocoupler.




**Working of optocoupler**

When an electrical signal is applied to the LED, the LED converts the electrical signal into an optical signal. The LED light falls on the photosensitive device and it converts the optical light into the electrical signal. (It generates the photocurrent) When light falls on the photo-sensitive device, it conducts and allows the flow of current. And the same current also flows through the external circuit which is connected with the photodetector.

In this way, the optocoupler optically couples the signal of one circuit to the other circuit.



**Applications of Optocoupler**

1. To isolate the two electrical circuits
2. Prevent very important low voltage circuits from noise, ground loops, and high voltage spikes
3. To control the high voltage circuit using a logic circuit or microcontroller (And yet keeping electrical isolation between them.
4. In communication Systems
5. Power Supplies
6. Solid-state Relays

## 3.5 Field Effect Transistor (FET)

**Q5. What is junction field effect transistor?**

*Ans :*

Junction field effect transistor (JFET) A junction filed effect transistor is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.

In a JFET, the current conduction is either by electrons (or) holes (unipolar). The JFET has high input impedance and low noice level.

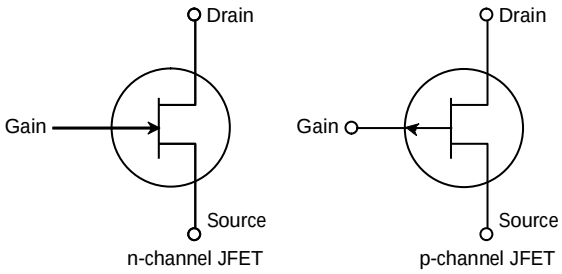



**Fig.: Schematic Symbol**

### 3.5.1 Types

**Q6. Define FET? Explain types of FET?**

*Ans :* **(Imp.)**

A field effect Transistor (FET) is a three terminal semiconductor device. Its operation is based on a controlled input voltage. By appearance JFET and bipolar transistors are very similar. However, BJT is a current controlled device and JFET is controlled by input voltage. Most commonly two types of FETs are available.

1. Junction field effect transistor (JFET)
2. Mental oxide Semiconductor FET (MOSFET)

**1. Junction field effect transistor (JFET)**

The functioning of junction filed effect transistor depends upon the flow of majority carriers (Electrons or wholes) only. Basically, JFETs consist of an N type (or) p-type silicon bar containing PN junctions at the sides. Following are some important points to remember about FET.

**Gate**

By using diffusion (or) alloying technique, both sides of N type bar are heavily doped to create PN junction. These doped regions are called gate (G).

**Source**

It is the entry point for majority carriers through which they enter into the semiconductor bar.

### Drain

It is the exit point for majority carrier through leave this semi conductor bar.

### Channel

It is the area of N type material through which majority carriers pass from the source to drain.

There are two types of JFET's commonly used in the field semiconductor devices. N-channel JFET and P-channel JFET.

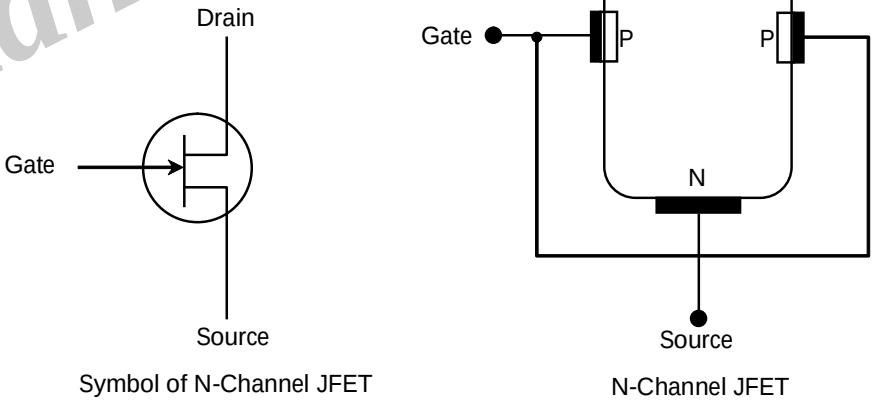
### N-Channel JFET

It has a thin layer of N-type material formed on p type substrate. Following shows the crystal structure and schematic symbol of an N-channel JFET. Then the gate is formed on top of the N channel with p type material. At the end of the channel and the gate, led wires are attached and the substrate has no connection.

When a DC voltage source is connected to the source and the drain leads of a JFET, maximum current will flow through the channel. The some amount of current will flow from the source and the drain terminal. The amount of channel current flow will be determined by the value of VDD and the internal resistance of the channel.

A typical value of source - drain resistance of a JFET is quite a few hundred ohms. It is clear that even when the gate is open full current conduction will take place is the channel. Essentially, the amount of bias voltage applied at ID, controls the flow of current carriers passing through the channel of a JFET. With a small change in gave voltage, JFET can be controlled any where between full conduction and cut off state.



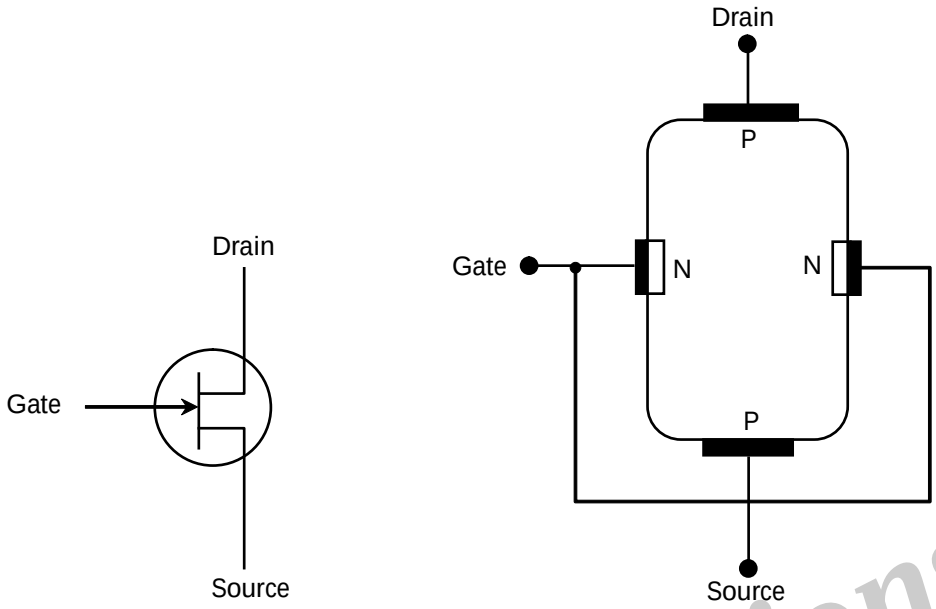



Symbol of N-Channel JFET N-Channel JFET

**Figure (a)**

### P-channel JFETs

It has a thin layer of p-type material formed on N type substrate. The following figure shows the crystal structure and schematic symbol of an N-channel JFET. The gate is formed on top of the p channel with N type material. At the end of the channel and the gate, lead wires are attached. Rest of the construction details are similar to that of N-channel JFET.



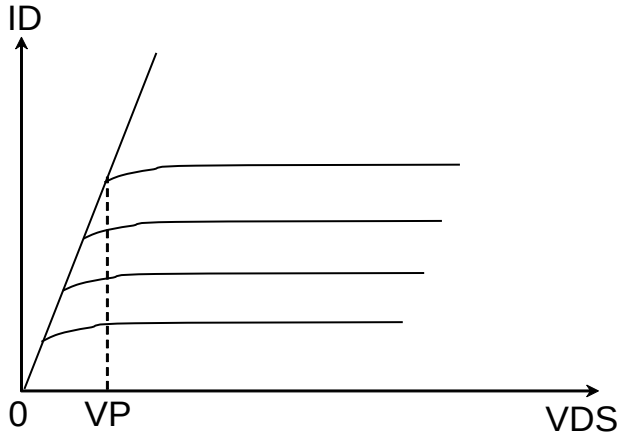

Symbol of P-Channel JFET P-Channel JFET

**Figure (b)**

Normally for general operation, the gate terminal is made positive with respect to the source terminal. The size of PN junction deplection layer depends upon fluctuations in the values of reverse biased gate voltage with a small change in gate voltage, JFET can be controlled anywhere between full conduction and cutoff state.

### Output Characteristics of JFET

The output characteristics of JFET are drawn between drain current ($I_D$) and drain source voltage ($V_{DS}$) at constant gate source voltage ($V_{GS}$) as shown in the following figure.




Initially, drain current (ID) rises rapidly with drain source voltage (VDS) however suddenly becomes constant at a voltage known as pinch-off voltage (VP), above pinch-off voltage, the channel width becomes so narrow that it allows very small drain current to pass through it. Therefore, drain current (ID) remains constant above pinch-off voltage.

### Parameters of JFET

The main parameters of JFET are

### AC drain resistance ($R_d$)

It is the ratio of change in the drain source voltage ($\Delta V_{DS}$) to the change in drain current ($\Delta$/D) at constant gate - source voltage. it can be expressed as,

$R_d = (\Delta_{VDS}) / (\Delta/D)$ at constant VGS

### Transconductance (gFs)

It is the ratio of change in drain current ($\Delta$/D) to the change in gate source voltage ($\Delta_{VGS}$) at constant drain source voltage. It can be expressed as,

$GFS = (\Delta/D)/V_{GS})$ at constant $V_{DS}$

### Amplification factor ($\mu$)

It is the ratio of change in drain source voltage ($\Delta$VDS) to the change in gate source voltage ($\Delta_{VGS}$) constant drain current ($\Delta$/D). It can be expressed as,

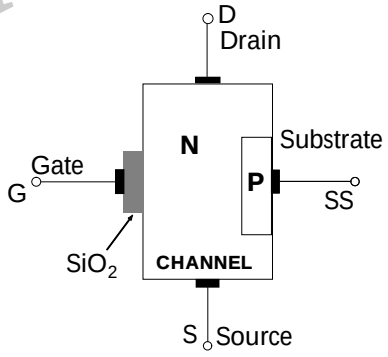
$U = (\Delta V_{DS}) / (\Delta_{VGS})$ at constant ID.

---

### Q7. What is MOSFET? Explain working and types of MOSFET?

*Ans :* **(Imp.)**

A MOSFET is a four-terminal device having source(S), gate (G), drain (D) and body (B) terminals. In general, The body of the MOSFET is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor. MOSFET is generally considered as a transistor and employed in both the analog and digital circuits. This is the basic introduction to MOSFET. And the general structure of this device is as below.

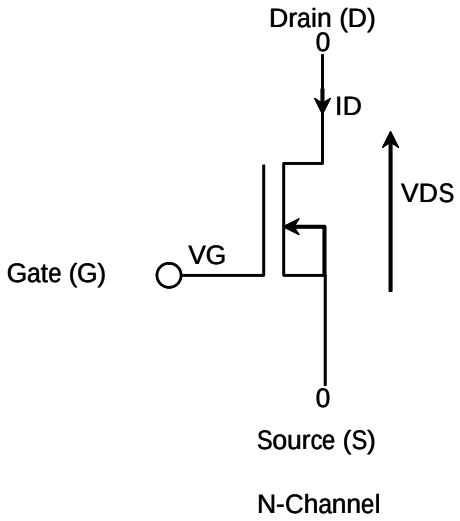


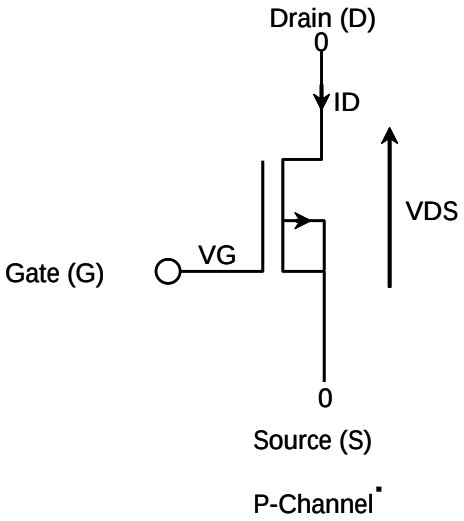

A MOSFET can function in two ways

- Depletion Mode
- Enhancement Mode

### Depletion Mode

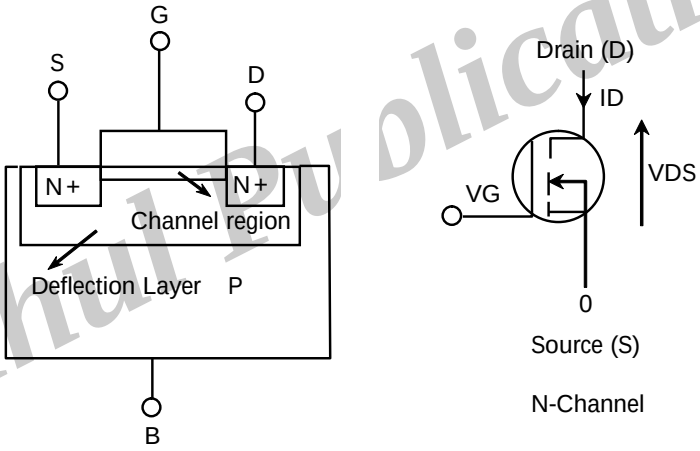
When there is no voltage across the gate terminal, the channel shows its maximum conductance. Whereas when the voltage across the gate terminal is either positive or negative, then the channel conductivity decreases.




**Enhancement Mode**

When there is no voltage across the gate terminal, then the device does not conduct. When there is the maximum voltage across the gate terminal, then the device shows enhanced conductivity.

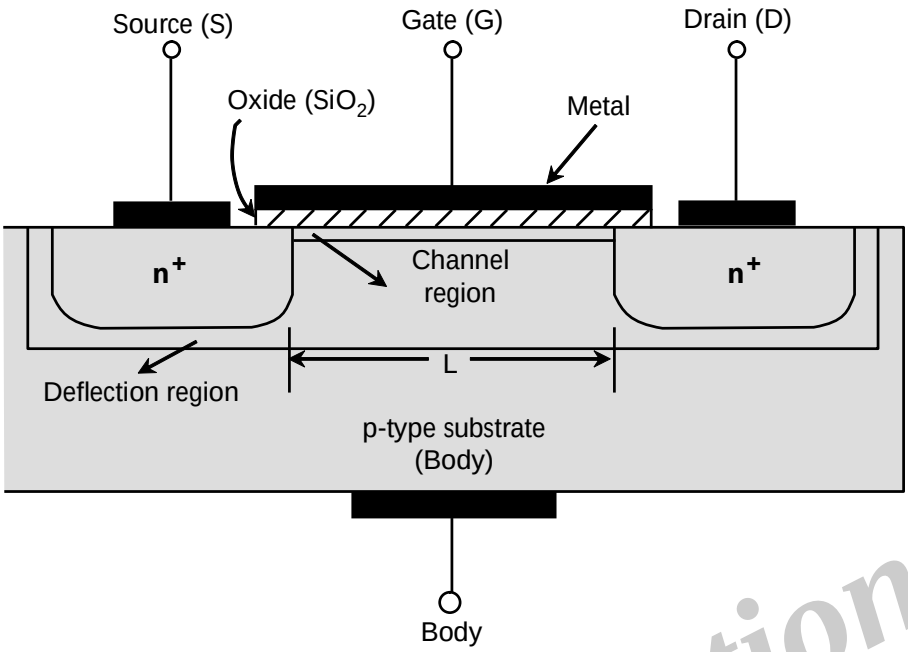



**Working Principle of MOSFET**

The main principle of the MOSFET device is to be able to control the voltage and current flow between the source and drain terminals. It works almost like a switch and the functionality of the device is based on the MOS capacitor. The MOS capacitor is the main part of MOSFET.

The semiconductor surface at the below oxide layer which is located between the source and drain terminal can be inverted from p-type to n-type by the application of either a positive or negative gate voltages respectively. When we apply a repulsive force for the positive gate voltage, then the holes present beneath the oxide layer are pushed downward with the substrate.

The depletion region populated by the bound negative charges which are associated with the acceptor atoms. When electrons are reached, a channel is developed. The positive voltage also attracts electrons from the n+ source and drain regions into the channel. Now, if a voltage is applied between the drain and source, the current flows freely between the source and drain and the gate voltage controls the electrons in the channel. Instead of the positive voltage, if we apply a negative voltage, a hole channel will be formed under the oxide layer.

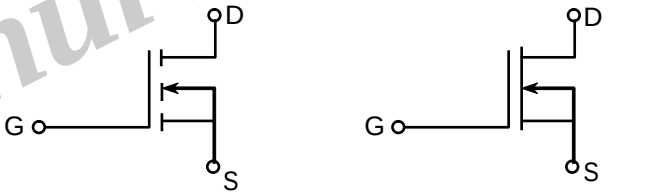



**MOSFET Block Diagram**

The N-channel MOSFETs are simply called as NMOS. The symbols for N-channel MOSFET are as given below.

**N-Channel MOSFET**

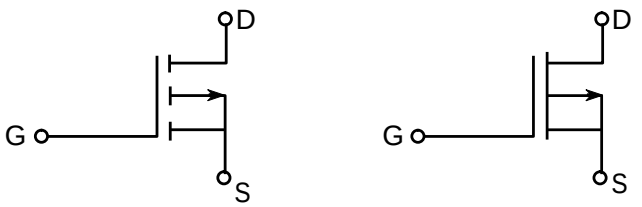
Symbols of N-Channel MOSFET




Enhancement Mode Depletion Mode

The P-channel MOSFETs are simply called as PMOS. The symbols for P-channel MOSFET are as given below.

Symbols of P-Channel MOSFET




Enhancement Mode Depletion Mode

## 3.6 FET AS AN AMPLIFIER

**Q8. Explain FET as an amplifier**

*Ans :*

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input Impedance. Because of high input impedance and other characteristics of JFETs they are preferred over

BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

i) Common Source

ii) Common Drain

iii) Common gain

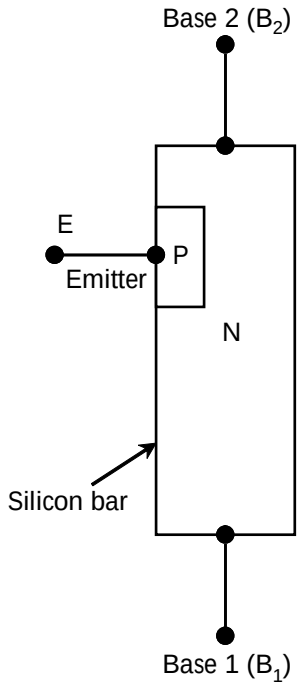
## 3.7 UNI JUNCTION TRANSISTOR (UJT)

**Q9. Explain the construction and working of UJT. Explain its characteristics.**

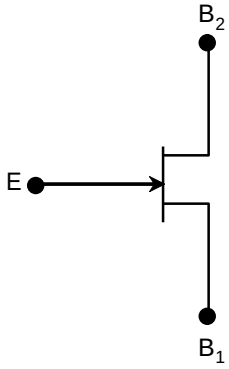
*Ans :* **(Imp.)**

**Construction**

UJT is an acronym for unijunction transistor. The basic structure of a unijunction transistor is as shown in figure (1). It contains a lightly doped N-type silicon bar on which a small portion of heavily doped p-type material is alloyed. The p-type material doped into N-type bar creates a single P-N junction. Because of this, it is known as unijunction. The N-type bar has two ohmic contacts at its ends named as base-1 ($B_1$) and base-2($B_2$) and the ohmic contact coming out of P-region is named as Emitter (E). As seen from figure (1), the emitter junction is created (or produced) closer to base-2 ($B_2$) than base-1($B_1$), So that the device is not symmetrical.



The symbol for Unijunction transistor is as shown in figure (2). The emitter leg is drawn in an single to the vertical line representing the N-type material slab and the arrow head points in the direction of conventional current when the device is forward biased, active or in the conducting state.




**Working**

The symbol and equivalent circuit of a UJT is as shown in figure below.

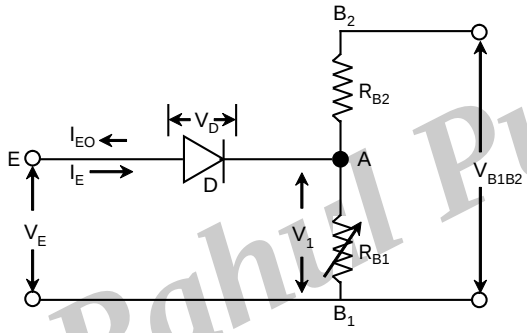



**Fig.: (a)**

When the voltage across the emitter terminal is zero, then the voltage VBB across the terminals $B_2$ and $B_1$ reverse biases the emitter diode. From figure (a), the total reverse bias voltage is,

$$V_A + V_B = \eta V_{BB} + V_B$$

Where, $V_B$ is the barrier voltage of the emitter diode. For silicon $V_B$ = 0.7 V.

Apply a Voltage $V_E$ across the emitter terminal and increase it slowly. The I flowing in the reverse biased diode reduces to zero When $V_E$ (voltage across emitter) become equal to $\eta V_{BB}$ that is,

When $V_E = n V_{BB+} I_{EO} = 0$

With equal voltage levels on each side of the diode, neither reverse nor forward current with flow.

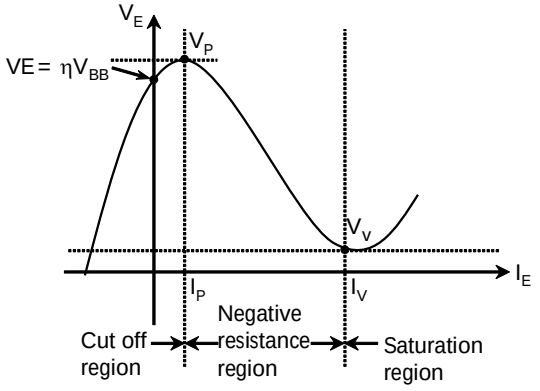
When the emitter supply voltage is increased further and exceeds the total reverse bias voltage $\eta V_{BB} + V_E$ the diode becomes forward - biased. The value of emitter voltage $V_E$ at which the diode becomes forwarded biased is called the peak-point voltage and is denoted by $V_p$. When $V_E = V_P$ emitter current IE starts flowing through $R_{B1}$ to ground, that is $B_1$.

This is the minimum current that is required to trigger the UJT. It is called peak-point emitter current and denoted by Ip. When the emitter diode starts conducting, charge carriers are injected into the $R_B$($R_{B1}$ = $R_{B2}$) region of the bar. Since the resistance of the semiconductor material depends upon doping, the resistance of $R_B$ region decreases rapidly due to additional charge carriers (holes). With the decrease in resistance, the voltage drop across RB also decreases causing the emitter diode to be more heavily forward biased. This, in turn results in larger forward current and consequently more charge carriers are injected causing still further reduction in the resistance of RB region. Thus the emitter current goes on increasing until it is limited by the emitter power supply. Since, the voltage at point A ($V_A$) decrease with increase in the emitter current, the UJT is said to have negative resistance characteristic.

It is seen that base - 2($B_2$) is used for only for applying external voltage $V_{BB}$ across it. Terminals E and $B_1$ are the active terminals. In general, UJT is triggered into conduction by applying a suitable positive pulse to the emitter. It can be turned off by applying a negative trigger pulse.

**V-I Characteristics of UJT**

The characteristics of UJT is a plot showing the relation between emitter voltage $V_1$ and emitter current $I_E$. It is shown n figure (a).



From figure (3), it is observed that $I_E$ never exceeds I for $V_E$ less than $V_P$. This region of the plot is called cut-off region. Once conduction is established at $V_E = V_P$ $V_E$ starts decreasing with increase in emitter current $I_E$. This region where $V_E$ decreases with increase in IE is known as negative resistance region of UJT. All applications of UJT use this region. Eventually, the valley point reaches, and any further increase in emitter current $I_E$ places the device in the saturation region.

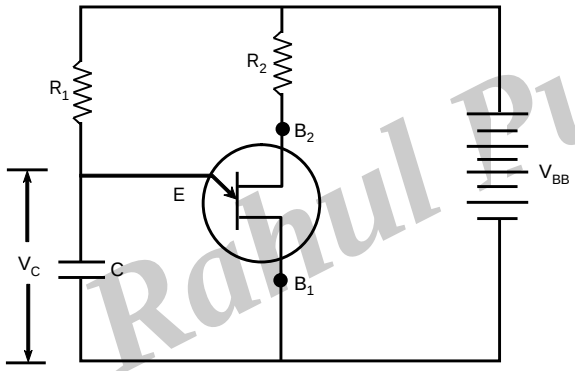
### 3.7.1 UJT as a Relaxation Oscillator

**Q10. Explain briefly UJT as a relaxation oscillation.**

*Ans :*

**UJT as a Relaxation Oscillator**

The circuit arrangement of UJT relaxation oscillator is shown in figure. It is specially used int he generation of sawooth waveform.




Here, the resistors $R_1$ and $R_2$ are the biassing resistors, the values of which are less than the internal base resistance $RB_1$ and $RB_2$. The value of resistor 'R1' is chosen in such a way tht the UJT operates in a negative resistance region.

The oscillating frequency is decided by the values of, $R_T$ and $C_T$.

**Functioning**

Initially, the UJT will be in cut-off region. Then the capacitor starts charging to the value of supply voltage through the resistor '$R_r$'. When the capacitor voltage reaches the peak voltage 'VP'. UJT starts conducting. The peak voltage is given by

Where,

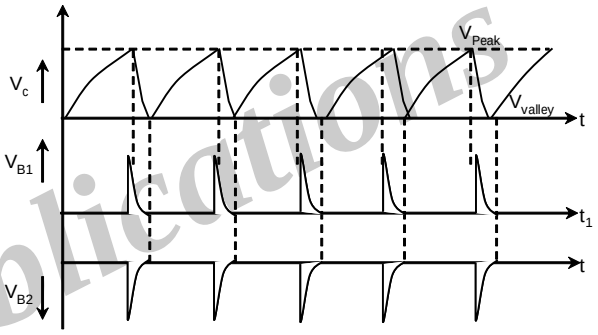
h – Stand - off ratio of UJT

VBB – Supply Voltage

VD – Cut in voltage (UJT)

When, the capacitor voltage goes beyond the peak voltage, capacitor starts discharging towards zero voltage reaches the zero volts, UJT goes into cut-off regions and again the capacitor starts charging.

The resistors $R_1$ and $R_2$ which are connected in series with base $B_1$ and $B_2$ produces spike signals. The sawtooth waveforms and spikes at $B_1$ and $B_2$ are shows in figure.




The charging equation of the capacitor is,

$$V_C = V_D + V_{SS}\,(1 - e^{-t/R_T C_T})$$

At $t = T$, $V_C = V_P$

Then, equation (1) becomes,

$$V_P = V_D + V_{BB}\,(1 - e^{-t/R_T C_T})$$

From, equation (1) substituting the value of 'in above equation, we get,

$$\eta\, V_{BB} + V_D = V_D + V_{SS}\,(1 - e^{-t/R_T C_T})$$

$$\eta = 1 - e^{-t/R_T C_T}$$

$$\therefore\ T = R_T\, C_T \ln\left(\frac{1}{1-\eta}\right)$$

$\therefore$ Frequency of oscillations,

$$f_0 = \frac{1}{T} = \frac{1}{R_T C_T \ln\left(\frac{1}{1-\eta}\right)}$$

**Q11. Draw two transistor representation of SCR. Mention two applications.**

*Ans :*

**Two-Transistor Representation**

Two-transistor model is used to explain the principle of operation of thyristor, Since, a thyristor is a four layered PNPN device, it can be considered as a combination of two transistors, one transistor as PNP and the other transistor as NPN.

Two-transistor model is obtained by separating the two middle layer of thyristor (as shown in figure (a)) two parts as shown in figure (b).

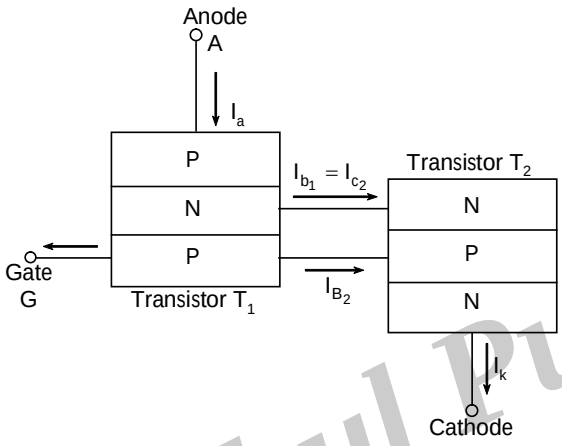



**Fig.: (a)**

In, this model, base current I of transistor $Q_1$ is equal to the collector current I of transistor Q1 and vice-versa equivalent circuit of two-transistor analogy is shown in figure (c).

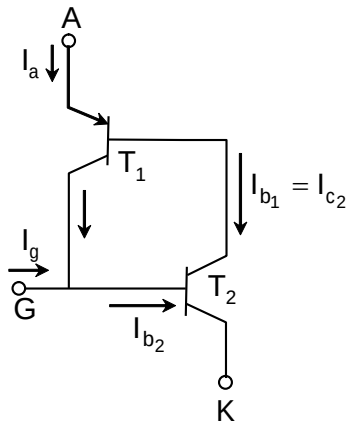



**Fig.: (b)**

**Applications**

The applications of SCR include,

1. Pulse control circuits
2. Zero point riggering circuits
3. Trigger circuits.
4. Crowbar circuit (or) Over voltage protection circuit.
5. High voltage applications

## 3.8 Silicon Controlled Rectifier

**Q12. Explain the construction and working N of SCR.**

*Ans :*

**Silicon Controlled Rectifier**

Silicon controlled rectifier is a four layered, three terminal device with three junctions namely J1, J2, and J3 as shown in figure. The End P-layer acts as node and end N-layer acts as cathode. A P-layer nearer to N-layer acts as gate. The circuit symbol of SCR is as shown in figure.

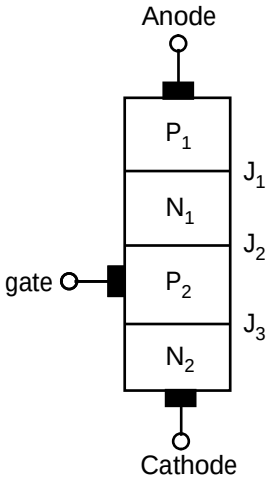



**Fig.: Basic Structure**

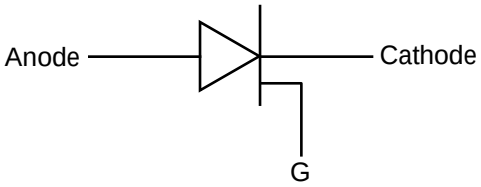



**Fig.: Circuit symbol**

The operation of silicon controlled rectifier is explained with the help of its characteristic.

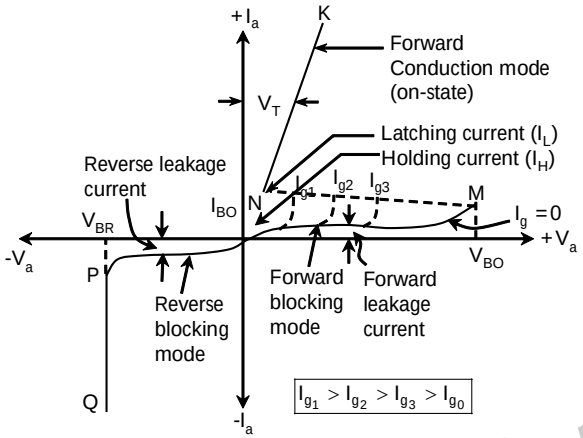
### V-I Characteristics of SCR

Figure illustrates the voltage - current characteristic of SCR. It has three modes of operation.

i) Forward blocking region

ii) Forward conduciton region

iii) Reverse blockign region.




### (i) Forward Block Region

In this region of operation, anode terminal is made positive wit respect tot he cathode and the gate terminal is open circuited (i.e., Ig = 0). In this mode of operation, junction J1 and J3 are forward biased and J2 is reverse biased. Due to depletion layer, at the junction J2 (gate), No. current flows through the circuit. But some small leakage current flows throught he circuit due to drift of mobile charge carriers. From the above point, it is clear that SCR is in forward biased condition but it does not conduct.

### (ii) Forward Conduction Region

If the applied voltage is increased further keeping gate terminal open circuited. Then the reversed biased junction J2 leads to avalanche breakdown and SCR turns into high conduction mode. The voltage at which junction J2 gets breakdown is known as forward break over voltage ($V_{BO}$). From the forward break over point SCR switches to on state. Once SCR started conducting means that the forward current is higher than minimum leakage current. The gate current is not required to maintain SCR in conducting state. The current at which he conduction of SCR starts is known as holding current ($I_H$).

### (iii) Reverse Blocking Region

When the cathode is mode positive with respect to the anode and open circuiting gate makes SCR to operate in reverse biased mode. The junction J1 and J3 are reverse biased and junction J2 is forward biased therefore small leakage current flows at junction 'J2' and that current is referred as reverse leakage current. If the reverse voltage is increased to reverse breakdown voltage an avalanche breakdown occurs at junction J1 and J3 and reverse current increases sharply. This region is referred as reverse blocking region.

## 3.8.1 SCR as a Switch

**Q12. Explain SCR as a switch?**

*Ans :*

The SCR has only two states, namely; ON state and OFF state in between. When appropriate gate current is passed, the SCR starts conducting heavily and remains in this position indefinitely even if gate voltage is removed. This corresponds to the ON condition. However when the anond current is reduced to the holding current, the SCR is turned OFF. It is clear tht behaviour of SCR is similar to a mechanical switch. As SCR is an electronic device, therefore, it is more appropriate to call it an electronic switch.

### Advantages of SCR as a switch

An SCR has following advantages over a mechanical or electromechanical switch (relay):

(i) It has no moving parts. Consequently, it give noiseless operation at high efficiency.

(ii) The switching sped is very high upto $10^9$ operations per second.

(iii) It permits control over large current (30 – 100 A) in the load by means of a small gate current (a few mA).

(iv) It has small size and gives trouble free service.

# Short Question and Answers

**1. Define FET?**

*Ans :*

A field effect transistor (FET) is a three terminal semiconductor device which can be used as an amplifier or switch. The three terminals are Drain (D), Source (S), and Gate (G).

**2. Compare BJT and MOSFET.**

*Ans :*

| S. No. | BJT | MOSFET |
|---|---|---|
| 1. | CB.CE.CC configurations | CS,CG,CD configurations |
| 2. | Less input resistance compared to JFET | Very high input resistance |
| 3. | Input output relation is linear | Input output relation is non-linear |
| 4. | Gain bandwidth product is high | Gain bandwidth product is low |
| 5. | Thermal noise is more | Thermal noise is less |
| 6. | Thermal stability is less | Thermal stability is more |
| 7. | Bigger size than MOSFET | Smaller size |

**3. What are the important features of FET?**

*Ans :*

- The parameters of FET are temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. Thus we can say FET is more temperature stable.
- FET has very high input impedance. Hence FET is preferred in amplifiers. It is less noisy.
- Requires less space.
- It exhibits no offset voltage at zero drain current.

**4. Define, Silicon Controlled Rectifier (SCR)?**

*Ans :*

A silicon controlled rectifier is a semiconductor device that acts as a true electronic switch. It can change alternating current into direct current and at the same time can control the amount of power fed to the load. Thus SCR combines the features of a rectifier and a transistor.

**5. What is the difference between BJT and FET? Explain each.**

*Ans :*

BJT is the short form of Bipolar Junction Transistor. FET is the short form of Field Effect Transistor. BJT is current controlled device while FET is voltage controlled device.

**Comparison between field Effect Transistor (FET) ANS Bipolar Junction Transistor (BJT).**

| Sl. No. | FET | BJT |
|---|---|---|
| 1. | It is a unipolar device. | It is a bipolar device |
| 2. | Its input resistance is very high. | Its input resistance is very low. |
| 3. | It is a voltage controlled device. | It is a current controlled device. |
| 4. | It has negative temperature coefficient at high current level. | It has positive temperature coefficient at high current level. |
| 5. | It does not suffer from minority carrier storage effects. | It suffers from minority carrier storage effects. |
| 6. | It has higher switching speed and cut off frequencies. | It has lower switching speed and cut off frequencies. |
| 7. | It is much simpler to fabricate as an integrated circuit. | It is more complicated to fabricate as an integrated circuit. |
| 8. | It is less noisy. | It is more noisy |
| 9. | It is relatively immune to radiation. | It is susceptible to radiation. |
| 10. | It has lower gain bandwidth product. | It has higher gain bandwidth product. |
| 11. | It requires special handling during installation. | It does not require special handling during installation. |

**6. Which parameters greatly affect the oscillator frequency in the UJT relaxation oscillator?**

*Ans :*

UJT relaxation oscillator

The oscillator frequency in the UJT relaxation oscillator depends upon the RC time constant circuit.

The time period of the relaxation oscillator is given by

$T = RC \log_e [ 1 / ( 1 - \eta )]$

(Where $\eta$ = Intrinsic stand off ratio).

**7. State the application of the UJT?**

*Ans :*

- Application
- Timing circuits
- Relaxation oscillators
- Trigger circuits
- Non sinusoidal oscillators
- Saw tooth generators
- Timing circuits.

**8. Explain classification of FET?**

*Ans :*

There are two main types of FET's. They are :

1. Junction Field Effect Transistor (JFET).
2. Insulated-gate Field Effect Transistor (IGFET) or (MOSFET).

These two, which is more commonly known as the standard metal oxide Semiconductor Field Effect Transistor (MOSFET).

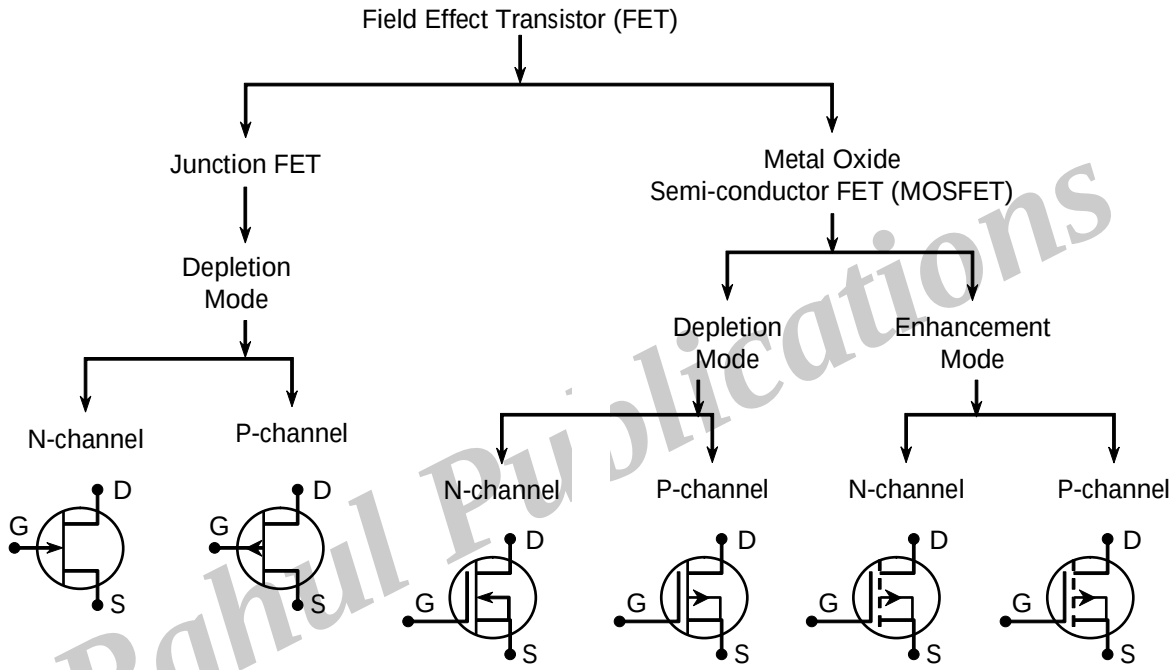



**Fig.: Types of JFETs and MOSFET's**



**9. Explain working principle of a solar cell?**

*Ans :*

Working Principle of a Solar Cell,

**1. Creation of electron-hole pairs**

When sufficient energy of light falls on the PN junction diode, the light can easily enter in the junction since the N-layer is very thin. This light energy creates a number of electron-hole pairs.

**2. Separation of electrons and Holes**

Due to this electron-hole pairs, there will be a great charqe gradient at the junction. Due to this built-in potential, the free electrons in the depletion region quickly come to the N-region. Similarly, the holes in the depletion region come to P region.

### 3. Collection of charge carriers

Because of this the concentration of electrons become more in N-region and concentration of holes become more in P-region. Therefore PN junction behaves like a small battery. These charges can be collected by the electrodes of the diode for practical use.

**Advantages**

1. No Pollution
2. Last for long life
3. No maintenance charges

**Disadvantages**

1. Cost of installation is high
2. Low efficiency
3. Can not be in the nights and cloudy days

**Applications**

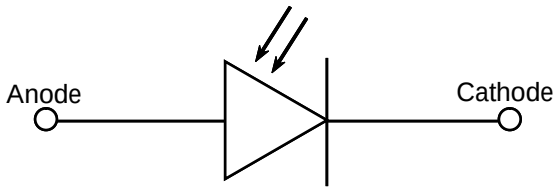
1. To charge the batteries
2. As a power generator
3. In calculators and wrist watches
4. In satellites ad spacecraft.

---

### 10. Define photodiode?

*Ans :*

Photodiode is a two terminal electronic device which, when exposed to light the current starts flowing in the diode. It is operated in reverse biased mode only. It converts light energy into electrical energy. When the ordinary diode is reverse biased the reverse current starts increasing with reverse voltage the same can be applied to the photodiode.




But in the case of photodiode the current can flow without application of reverse voltage, the P-N junction of the photodiode is illuminated by light and light energy dislodge valence electrons and the diode starts conducting.

# Choose the Correct Answers

1. FET is _____ control device. [ b ]
   (a) Current (b) Voltage
   (c) Power (d) Both a and b
2. A FET has [ a ]
   (a) Very high i/p impedance (b) Very low input impedance
   (c) Very low gain (d) All of the above
3. JFET is _____ device [ b ]
   (a) Bipolar (b) Unipolar
   (c) Multipular (d) Both a and b
4. Optocoupler is also known as [ b ]
   (a) Opto (b) Optoisolator
   (c) Diaopto (d) None of the above
5. JFT can be used as _____ resistor [ a ]
   (a) Voltge variable (b) Current variable
   (c) Both a and b (d) None of the above
6. An SCR has [ d ]
   (a) One layer (b) Two layer
   (c) Three layer (d) Four layer
7. The number of PN Juncitons is SCR is [ a ]
   (a) 3 (b) 2
   (c) 4 (d) 5
8. In photo didoe, the light signals are converted into _____ signals. [ c ]
   (a) Chemical (b) Mechanical
   (c) electircal (d) None of the above
9. An LED can be made from. [ a ]
   (a) Germanium (b) Silcon
   (c) Gallium Arsenide (d) Phosphorescent material
10. Solar cell works on the principle of [ b ]
   (a) Photo cell (b) Photovoltaic cell
   (c) Batteries (d) None of the above

# Fill in the Blanks

1. LED emits _____.
2. The SCR resembles the _____ electrically.
3. The dark current is photo diode is due to _____.
4. A photo didoe is _____.
5. JFET behaves as _____ for small values of drain to source voltage.
6. The UJT is operated as _____ in negative resistance region.
7. Relation between $\mu$, $r_d$ and $g_{as}$ is _____.
8. _____ is grown over the surface of MOSFET as an insulating layer.
9. FET acts as voltage variable resistor at _____ region.
10. UJT is generally is used for _____.

## ANSWERS

1. Light
2. Diode
3. Thermally generated minority carriers
4. Phot detector
5. Resistor
6. Oscillator
7. $m = g_{as}\ r_d$
8. $Sio_2$
9. Ohmic
10. Sawtooth wave generation.

UNIT IV

**Digital Electronics:**
Binary number system, convertion of binary to decimal and vice-versa. Binary addition and subtraction (I's and 2's complement methods). Hexadecimal number system. Conversion from binary to hexadecimal and vice-versa, Decimal to hexadecimal and vice-versa.

**Logic gates:**
OR, AND, NOT gates, truth tables, realization of these gates using discrete components. NAND, NOR as universal gates, Exclusive – OR gate (EX-OR). De Morgan's Laws - Verification.

## 4.1 Binary Number System

**Q1. What is binary number system? Explain with suitable example.**

*Ans :*

A system that represents a number with a combination of only two digits i.e., '0' and '1' is known as binary number system. In this system, each binary digit is referred as 'bit'. The base/ radix of a binary number is '2'.

For example, a binary number is represented as $(1101001)_2$ and the weight / value of each bit is expressed as a power of '2'. The left most bit process largest weight and is termed as most significant bit (MSB). Similarly, the right most bit possess smallest (or) least weight and is known as least significant bit (LSB). Any binary number can be converted into decimal number by adding all the bits multiplied by their weights. Table (2) shows the binary bits their weights expressed in powers of 2.

| Position | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|---|---|---|
| Digit | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| Weight | $1\times2^6$ | $1\times2^5$ | $0\times2^4$ | $1\times2^6$ | $0\times2^2$ | $0\times2^1$ | $1\times2^0$ |
| | | MSB | | | | | LSB |

i.e., $1101001 = (1 \times 2^6) + (1 \times 2^5) + (0 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + k\,(0 \times 2^1) + (1 \times 2^0)$

$= 64 + 32 + 0 + 8 + 0 + 0 + 1 = 105$

$\therefore \quad (1101001)_2 = (105)_{10}$

## 4.2 Binary to Decimal Conversion

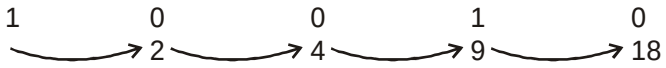
**Q2. Explain converting of binary to decimal.**

*Ans :* **(Imp.)**

**(i) Conversion of integral binary numbers**

A more popular way to convert integral binary number to decimal numbers is the double-and-add method. In this method. In this method we start from the most significant bit, double the 1 present in that bit and proceed to the next bit. If next bit is 0, double the number obtained in the previous step; If it is 1, add a 1 after double. The process is repeated until the least significant bit has been proceed.

As an example, let us convert 100100 to its equivalent decimal number.




double 1 × 2 = 2 double 2 × 2 = 4 double 4 × 2 + 1 = 9 9 × 2 = 18 and add

Thus binary 10010 = decimal 18

i.e., $10010_2 = 18_{10}$

**(ii) Conversion of fractional binary numbers**

In order to convert the binary fraction to equal decimal numbers, we note the weights are,

Binary point
or, in powers of 2

$\frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \frac{1}{16}$ etc

Binary point

$2^{-1}, 2^{-2}, 2^{-3}, 2^{-4}$, etc

As an example, let us find the decimal equivalent of 0.1101.

$$0.1 \quad 1 \quad 0 \quad 1$$

$$= \frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{1}{16}$$

$$= .5 + .25 + 0 + .0625$$

$$= 0.8125$$

For mixed numbers, that is, having integer and fractional parts, each part is handled separately according to the rules just developed. Thus the decimal equivalent of 10010.1001 is 18.8125 because the decimal equivalent of 10010.1101 is 18.8125 because the decimal equivalent of 10010 is 18 and that of .1101 is 8125 as discussed above.



### 4.2.1 Decimal Number System

**Q3. What is decimal number system?**

*Ans :*

A number system that represents a combination of algebraic numerals (i.e., 0,1,3,4,5,6,7,8,9) is termed as decimal number system. In system, any decimal number can be expressed in units, tens hundreds, thousands, lakhs, and So on. For example, a decimal number 4318 is read as 'Four thousand three hundread and eighteen and can be represented as,

$4318 = (4 \times 1000) + (3 \times 100) + (1 \times 10) + (8 \times 1)$

The decimal number can also be represented as $(4318)_{10}$. The subscript '10' denotes the base (or) radix of the number. The value/weight of each digit is obtained by its position. The left most digit possess

large weight and is known as most significant digit (mSD). Similarly, the right most digit possess least (or) smallest weight and is termed as least significant digit(LSD). Table below shows the decimal digits with their weights expressed in power of 10.

| Position | $10^3$ | $10^2$ | $10^1$ | $10^0$ |
|---|---|---|---|---|
| Digit | 4 | 3 | 1 | 8 |
| Weight | $4\times10^3$ | $3\times10^2$ | $1\times10^1$ | $8\times10^0$ |
| | MSD | | | LSD |

## 4.3 Decimal to Binary Conversion

**Q4. Explain converting of decimal to binary conversion.**

*Ans :* **(Imp.)**

**(i) Conversions of integral decimal numbers**

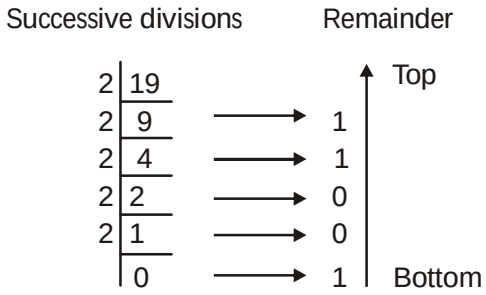
A general method for converting integral decimal numbers to binary system

| Divide by 2 | 0 | 1 | 2 | 5 | 10 | 21 decimal |
|---|---|---|---|---|---|---|
| Remainder | 1 | 0 | 1 | 0 | 1 | Binary |

$$10101 = 1\times2^4 + 0\times2^3 + 0\times2^2 + 0\times2^1 + 0\times2^0$$

$$= 16 + 0 + 4 + 0 + 1 = 21$$

This method can be explained in a slightly different manner as shown below where the decimal number 19 is converted into its binary equivalent.




Reading the remainder from the bottom to the top, the binary equivalent of 19 is found to be 10011, (or) $19_{10} = 10011_2$.

**(ii) Conversion of fractional-decimal numbers**

This method of converting numbers to binary number is called the double-dabble method.

As an example let us convert 0.638 to binary from

| | Binary |
|---|---|
| 0.638 × 2 = 1.276 | 1 |
| 0.276 × 2 = 0.552 | 0 |
| 0.552 × 2 = 1.104 | 1 |
| 0.104 × 2 = 0.208 | 0 |
| 0.208 × 2 = 0.416 | 0 |
| 0.416 × 2 = 0.832 | 0 |
| 0.832 × 2 = 1.664 | 1 |
| 0.664 × 2 = 1.328 | 1 |
| 0.328 × 2 = 0.656 | 0 |
| 0.656 × 2 = 1.656 | 1 |

Rounding off after 10 bits (which has introduced an error of less than $2^{-10}$), then binary result is,

Decimal 0.638 = binary 0.1010001101

(or) $0.638_{10} = 0.1010001101_2$

## 4.4 BINARY ADDITION

**Q5. Explain binary addition.**

*Ans :*

Binary addition is very simple and can be made with the four rules :

1) 0 + 0 = 0

   i.e., when nothing is added to nothing, we get nothing

2) 0 + 1 = 1

   i.e., when nothing is added to one, we get one

3) 1 + 0 = 1

   i.e., when one is added to nothing, we get one. This is just reverse of case (2).

4) 1 + 1 = 10 (One - zero, not ten

   i.e., when one is added to one, we get two because decimal equivalent of 10 (one - zero) is 2.

The last rule is often written as

1 + 1 = 0 with a carry of 1.

The addition of two binary number A and B can also be expressed in the form a truth table shown below :

| Inputs | | Sum | Carry |
|---|---|---|---|
| A | B | | |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

As an example, let us add binary 101(5) to 110(6), where bracted numbers represent the decimal equivalents.

| | | | | | |
|---|---|---|---|---|---|
| | 1 | 0 | 1 | – First column | : 1 + 0 = 1 |
| + | 1 | 1 | 0 | – Second column | : 0 + 1 = 1 |
| 1 | 0 | 1 | 1 | – Third column | : 1 + 1 = 0 |
| | | | | | (i.e., 0 with a carry 1) |

## 4.5 BINARY SUBSTRACTION

**Q6. Explain binary substraction.**

*Ans :*

The four rules of binary substraction are given below :

1. 0 – 0 = 0
2. 1 – 0 = 0
3. 1 – 1 = 0
4. 10 – 1 = 1

The last rule indicates that when 1 is substracted from $10_2$ (= decimal 2).

| Inputs | | Outputs | |
|---|---|---|---|
| A | B | Sum | Carry |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

As an example; let us substract binary 10001(17) from 10011(19) where bracketed numbers represent the equivalent decimal numbers. Then

| | | | | | |
|---|---|---|---|---|---|
| | 1 | 0 | 0 | 1 | 1 |
| – | 1 | 0 | 0 | 0 | 1 |
| | 0 | 0 | 0 | 1 | 0 |

## 4.6 Complement of a Number

### 4.6.1 1's & 2's Complement of binary addition

**Q7. Explain 1's & 2's complement of binary addition.**

*Ans :*

The usual practice in computers is to change the substraction to an addition process. Thus the circuity is simplified because only adder circuits are needed for both addition and substraction.

In digital work, two types of complements of a binary number are used.

**(a) 1's complement**

The 1's complement of a binary number is the number which is obtained by changing its each 0 into a 1 and each 1 into a 0. For example, 1's complement of the binary number 1011 is 0100, and of 10011 is 01100.

**(b) 2's complement**

The 2's complement of a binary number is the number which is obtained by adding 1 to its 1's complement.

Thus,

2's complement = 1's complement + 1

Thus the 2's complement of binary number 1011 is 0100 + 1 = 0101.

The following table gives is and 2's complements of some binary numbers.

| Binary number | 1's complement | 2's complement |
|---|---|---|
| 100 | 011 | 100 |
| 101 | 010 | 011 |
| 1010 | 0101 | 0110 |
| 1011 | 0100 | 0101 |
| 1110 | 0001 | 0010 |
| 10100 | 01011 | 01100 |



### 4.6.2 1's Complement of binary substraction

**Q8. Explain 1's complement of binary substraction.**

*Ans :*

Substraction of binary numbers using one's complement method:

In one's complement substraction method, the subtrahend is represented in One's complement from and added to the minuend.

For example, in the calculation of 'x – y' using one's complement method, One's complement of 'y' is added to 'x' .

**Procedure**

**Step - 1:**

The first step is to find the one's complement of substrahend (or) negative number.

**Step - 2:**

The next step is to add the one's complement of substrahend to the minuend (or) positive number.

**Step - 3:**

If any carry is produced in step-2, it indicates the positive result. This carry is added to LSB of the partial result. On the other hand, if carry is not produced in step-2, it indicates the negative result. To obtain the actual result, the partial result is converted to its one's complement form and negative sign is assigned at the beginning.

**Example 1:**

Perform $(34)_{10} - (25)_{10}$ using 1's complement representation.

Binary representation of 34 is 100010

Binary representation of 25 is 011001

$(34)_{10} - (25)_{10} = (100010)_2 - (011001)_2$

Here, substrahend = 011001

minuend = 1000101

**Step - 1:**

1's complement of substrahend (i.e., 011001) is 100100

**Step - 2:**

Add is complement of '011001' to '100010' (1) (1) carry

100010 minuend (Binary equivalent of $(34)_{10}$)

100110 1's complement of subtrahend $(-25)_{10}$

carry (1) 001000 partial result

**Step - 3:**

The carry obtained in the partial result specifies that it is a positive numbers. The final result is obtained by adding carry to the LSB of partial result as

0 0 1 0 0 0

\+ +

0 0 1 0 0 1 Final result

**Example 2:**

Perform $(25)_{10} - (34)_{10}$ using is complement representation.

$(25)_{10} - (34)_{10} = (0110001)_2 - (100010)_2$

Here,

subtrahend = 100010

minuend = 011001

**Step - 1:**

One's complement of subtrahend

(i.e., 100010) is 011101

**Step - 2:**

Add 1's complement of 100010 to 011001

(1) (1) (1) carry

0 111 00 1 minuend (Binary equivalent of $(25)_{10}$)

+ 011 00 1 1's complement of substrahend $(-34)_{10}$

1 10110 partial result

**Step - 3:**

The absence of carry in the partial result specifies that it is a negative number. The final result is obtained by taking 1's complement of partial result.

i.e., 001001 (Final result)

$\therefore \quad (25)_{10} - (34)_{10} = -(001001)_2 = (-9)_{10}$

### 4.6.3 2's Complement of binary substraction

**Q9. Explain 2's complement of binary substraction.**

*Ans :*

In two's complement substraction method, the substrahend is represented in two's complement form and added to the minuend. For example, in the calculation of 'x – y' using two's complement method 2's complement of 'y' is added to 'x'.

**Procedure**

**Step - 1:**

Find the two's complement of substrahend (or) negative number.

**Step - 2:**

Add the two's complement of substrahend to the minuend (or) positive number.

**Step - 3:**

If carry is produced in step-2, it indicates the positive result and the carry is neglected. On the other hand if carry is not produced in step-2, it indicates the negative result. The actual result can be obtain by taking the 2's complement of partial result and placing negative sign before it.

**Complement substraction**

1. Substraction of smaller number from larger number method.
   (i) First determine the 2's complement of the smaller number.
   (ii) The 2's complement so obtained is added to the larger number.
   (iii) Discard the carry if any.

**Example 1:**

Perform $(26)_{10} - (14)_{10}$ using 2's complement representation

Binary representation of 25 is 011010

Binary representation of 14 is 001110

$(26)_{10} - (14)_{10} = (011010)_2 - (001110)_2$

Here,

substrahend = 001110

minuend = 011010

**Step - 1:**

Find the 2's complement of substrahend.

| | |
|---|---|
| 0 0 1 1 1 0 | Subtrahend |
| (1) | |
| 1 1 0 0 0 1 0 | 1's complement of substrahend |
| +1 | Adding 1 to 1's complement to get 2's complement |
| 1 1 0 0 1 0 | 2's complement of substrahend |

**Step - 2:**

Add 2's complement of '001110' to '011010'

| | |
|---|---|
| 0 1 1 0 1 0 | minuend [binary equivalent of $(26)_{10}$] |
| 1 1 0 0 1 0 | 2's complement of substrahend $(-14)_{10}$ |
| 1 0 0 1 1 0 | Partial result |

(1) carry

**Step - 3:**

The carry obtained in the partial result specifies that it is a positive number.

Neglect the carry (1) to obtain the final result,

i.e., $001100 = (12)_{10}$

$\therefore \quad (26)_{10} - (14)_{10} = (01100)_2 = (12)_{10}$

2. Substraction of larger number from smaller number method

(i) First, determine the 2's complement of the larger number.

(ii) The 2's complement so obtained is added to the smaller number.

(iii) The resultant will be in the 2's complement form. In order to obtain answer in the true form, the 2's complement of the answer is taken and a negative sign is assigned to it.

**Example 2:**

Perform $(14)_{10} - (26)_{10}$ using 2's complement representation

i.e., $(14)_{10} - (26)_{10} = (001110)_2 - (011010)_2$

Here,

substrahend = 011010

minuend = 001110

**Step - 1:**

Find the 2's complement of subtrahend,

| | |
|---|---|
| 0 1 1 0 1 0 | subtrahend |
| (1) | |
| 1 0 0 1 0 1 | 1's complement of substrahend |
| + 1 | Adding 1 to 1's complement to get 2's complement of substrahend |
| 1 0 0 1 1 0 | 2's complement of substrahend |

**Step - 2:**

Add 2's complement of '011010' to '001110'

| | |
|---|---|
| 0 0 1 1 1 0 | minuend [Binary equivalent of $(14)_{10}$] |
| + 1 0 0 1 1 0 | 2's complement of substrahend $(-26)_{10}$ |
| 1 1 0 1 0 0 | Partial result (No carry is generated) |

**Step - 3:**

The absence of carry in the partial result specified that it is a negative number. The final result is obtained by taking 2's complement of partial result

| | |
|---|---|
| 1 1 0 1 0 0 | Partial result |
| (1) | |
| 0 0 1 0 1 1 | 1's complement |
| + 1 | Adding 1 to 1's complement |
| 0 0 1 1 0 0 | Final |

$\therefore$ $(14)_{10} - (26)_{10} = (001100)_2 = (-12)_{10}$

## 4.7 Conversion from Binary to Hexadecimal

**Q10. Explain converting form binary to Hexadecimal.**

*Ans :* **(Imp.)**

A system that represents a number with the combination of 16 digits i.e., 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E and F is known as hexadecimal number system.

As the hexadecimal number system used 16 digits, the base / radix of hexadecimal number is 16. table. Shows the relationship between decimal, binary and hexadecimal number system.

| Decimal | Binary | Hexadecimal |
|---|---|---|
| 0 | 000 | 0 |
| 1 | 001 | 1 |
| 2 | 0010 | 2 |
| 3 | 0011 | 3 |
| 4 | 0100 | 4 |
| 5 | 0101 | 5 |
| 6 | 0110 | 6 |
| 7 | 0111 | 7 |
| 8 | 1000 | 8 |
| 9 | 1001 | 9 |
| 10 | 1010 | A |
| 11 | 1011 | B |
| 12 | 1100 | C |
| 13 | 1101 | D |
| 14 | 1110 | E |
| 15 | 1111 | F |

For example, consider the binary number 10110101111011.

The binary number is splitted into 4 bit groups as

0010 1101 0111 1011

Each group is replaced with its equivalent hexadecimal number as,

0010 1101 0111 1011

↓ ↓ ↓ ↓

2 D 7 8

$\therefore \quad (10110101111011)_2 = (2D7B)_{16}$

## 4.8 Conversion from Hexadecimal to Binary

**Q11. Explain converting from hexadecimal to binary.**

*Ans :*

A hexadecimal number can be converted into binary number by replacing each digit with its binary equivalent. For example, consider the hexadecimal number (2B9D).

Each digit is converted into equivalent binary number as,

| 2 | B | 9 | D |
|---|---|---|---|
| ↓ | ↓ | ↓ | ↓ |
| 2 | D | 7 | 8 |

$\therefore \quad (2B9D)_{16} = (0010101110011101)_2$

## 4.9 HEXADECIMAL TO DECIMAL

**Q12. Explain converting hexadecimal to decimal.**

*Ans :*

To convert from hexadecimal to decimal we put the value of each digit from Table of sec. 1019, then multiply each digit by its weight and add the resulting products.

To explain, consider an example to convert $3C8_{16}$ to its decimal equivalent. Then

$$3C8_{16} = 3 \times 16^2 + 12 \times 16^1 + 8 \times 16^0$$

$$= 768 + 192 + 8 = 968_{10}$$

Here we have replaced C by decimal 12 from table of section.

Consider, another example to convert $E5F_8$ to decimal.

$$E5F8_{16} = 14 \times 16^3 + 5 \times 16^2 + 15 \times 16^1 + 8 \times 16^\circ$$

$$= 57344 + 1280 + 240 + 8$$

$$= 58,872_{10}$$

**Q13. Explain converting decimal to hexadecimal.**

*Ans :*

For it a hex-dabble method is used in which, a decimal number is successively divided by 16. The remainders are converted to hex notations and read in the reverse order i.e., from bottom to top.

**For example:** Convert $72905_{10}$ to hexadecimal.

Then

| Successive Division | Remainder | Hexnotations |
|---|---|---|
| 16 \| 72905 | 9 | 9 ↑ |
| 16 \| 4556 | 12 | C |
| 16 \| 284 | 12 | C |
| 16 \| 17 | 01 | 1 |
| 16 \| 1 | 01 | 1 |
| 0 | | |

Reading the remainders from bottom to top, the result is $11CC9_{16}$. Thus

$$72905_{10} = 11CC9_{16}$$

Consider another example to convert $423_{10}$ to hexadecimal. 16 1423

| | | | |
|---|---|---|---|
| 16 | 423 | 7 | 7 ↑ |
| 16 | 26 | 10 | A |
| 16 | 1 | 1 | 1 |
| | 0 | | |

Thus, $423_{10} = 1A7_{16}$

## PROBLEMS

**1 1001 convert binary to hexadecimal.**

*Sol :*

Given binary number is, 1001.

Conversion of binary number into its hexadecimal number, the number is first divided into a group of four from LSB to MSB. In case at the MSB if there are no sufficient bits to form a group of four bits then, zeros are added and complete four bits group is formed. Each group is then replaced with its equivalent hexadecimal number.

i.e.,

1001
↓
9

$\therefore \quad (1001)_2 = (9)_{16}$

**2 101010 binary to hexadecimal.**

*Sol :*

Given binary number is 101010

| 0010 | 1010 |
|---|---|
| 2 | 10 |
| ↓ | ↓ |
| 2 | A |

i.e.,

$\therefore \quad (101010)_2 = (2A)_{16}$

**3. 10101100 convert binary to hexadecimal.**

*Sol :*

Given binary number is, 10101100

| 1010 | 1100 |
|---|---|
| ↓ | ↓ |
| 12 | 14 |
| ↓ | ↓ |
| A | C |

i.e.,

$\therefore \quad (10101100)_2 = (2AC)_{16}$

---

**4. 4236 convert binary to hexadecimal.**

*Sol :*

Given hexadecimal number is, 4236.

Conversion of Hexadecimal number into binary numbers.

The given hexadecimal number can be converted into binary number by replacing each digit with its binary equivalent as,

| 4 | 2 | 3 | 6 |
|---|---|---|---|
| ↓ | ↓ | ↓ | ↓ |
| 0100 | 0010 | 0011 | 0110 |

$\therefore \ (4236.6)_{10} = (0100001000110110)_2$

---

**5. AB6.13 convert binary to hexadecimal.**

*Sol :*

Given hexadecimal number is, AB6.13

Conversion of hexadecimal number into binary number.

Given hexadecimal number can be converted into binary equivalent as,

| A | B | 6 | 1 | 3 |
|---|---|---|---|---|
| ↓ | ↓ | ↓ | ↓ | ↓ |
| 1010 | 1011 | 0110 | 0001 | 0011 |

$(AB6.13)_{16} = (101010110110.00010011)_2$

**6. 115 convert decimal to hexadecimal.**

*Sol :*

Given decimal number is, 115

Conversion of decimal number into hexadecimal number,

$$\begin{array}{r|l} 16 & 115 \\ 16 & 7-3 \uparrow \\ & 0-7 \end{array}$$

$\therefore \quad (115)_{10} = (73)_{16}$

---

**7. 235 convert decimal to hexadecimal.**

*Sol :*

Given decimal number, is 235

conversion of decimal number into hexadecimal number

$$\begin{array}{r|l} 16 & 235 \\ 16 & 14-11 \uparrow \text{B} \\ & 0-14 \quad\quad \text{E} \end{array}$$

$\therefore \quad (235)_{10} = (EB)_{16}$

---

**8. $(5B8E)_{16}$ into decimal system**

*Sol :*

Given hexadecimal number is, 5B8E

**Step - 1:**

Conversion of hexadecimal to binary equivalent

The binary form of the hexadecimal number 5B8E is

0101 1011 1000 1110

**Step - 2:**

Conversion of binary to decimal

The decimal form of the obtained binary number is,

| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

$= (1\times2^{14}) + (1\times2^{12}) + (1\times2^{11}) + (1\times2^9) + (1\times2^8) + (1\times2^7) + (1\times2^3) + (1\times2^2) + (1\times2^1)$

$= 16384 + 4096 + 2048 + 512 + 256 + 128 + 8 + 4 + 2$

$= 23438$

**9. $(5B6E)_{16}$ convert into decimal form.**

*Sol :*

Given hexadecimal number is, $5B6E_{16}$

**Step - 1:**

Conversion of hexadecimal to binary equivalent.

The binary form of the hexadecimal number 5B6E is

0101101101101110

**Step - 2:**

Conversion of binary to decimal

The decimal form of the obtained binary number is,

| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

$= (1\times2^{14}) + (1\times2^{12}) + (1\times2^{11}) + (1\times2^9) + (1\times2^8) + (1\times2^6) + (1\times2^5) + (1\times2^3) + (1\times2^2)$

$+ (1\times2^1)$

$= 16384 + 4096 + 2048 + 512 + 256 + 64 + 32 + 4 + 2$

$= 23,406$

$\therefore \quad (5B6E)_{16} = (23406)_6$

**10. $(3A45)_{16}$ convert into decimal form.**

*Sol :*

Given hexadecimal number, is, 3A45

**Step - 1:**

Conversion of hexadecimal to binary equivalent

The binary form of the hexadecimal number 3A45 is,

001110 10 0100 01 01

**Step - 2:**

Conversion of binary to decimal

The decimal form of the obtained binary number is,

| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^9$ | $2^8$ | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |

$= (1\times2^{13}) + (1\times2^{12}) + (1\times2^{11}) + (1\times2^9) + (1\times2^6) + (1\times2^2) + (1\times2^0)$

$= 8195 + 4096 + 2048 + 512 + 64 + 4 + 1$

$= 14,917$

$\therefore \quad (3A45)_{16} = (14,917)_{10}$

**11. 214 convert decimal to hexadecimal.**

*Sol :*

Given decimal number is 214

$$\begin{array}{r|l} 16 & 214 \\ 16 & 13-6 \\ & 0-13 \end{array}$$

$\therefore \quad 214 = (136)_{16} = (D6)_{16}$

**12. 5625 convert decimal to hexadecimal.**

*Sol :*

Given decimal number is 5625

$$\begin{array}{r|l} 16 & 5625 \\ 16 & 351-9 \\ 16 & 21-15 \\ 16 & 1-5 \\ & 0-1 \end{array}$$

$\therefore \quad 5625 = (15159)_{16} = (15F9)$

**13. 157 convert decimal to hexadecimal.**

*Sol :*

Given decimal number is, 157

$$\begin{array}{r|l} 16 & 157 \\ 16 & 9-13 \\ & 0-9 \end{array}$$

$\therefore \quad 157 = (913)_{16} = (9D)_{16}$

**14. $(1001001)_2$ binary to hexadecimal.**

*Sol :*

Given binary number is, $(1001001)_2$

$$\begin{array}{c:c} 0100 & 0100 \\ 4 & 9 \end{array}$$

$\therefore \quad (1001001)_2$

**15. $(1110110)_2$ convert binary to hexadecimal.**

*Sol :*

Given binary number is $(1110110)_2$

| 0111 | 0110 |
|---|---|
| 7 | 6 |

$\therefore \quad (1110110)_2 = (76)_{16}$

## 4.10 Logic Gates

### 4.10.1 NOT, AND, OR, NANO, NOR truth tables

**Q14. What are logic gates? Explain about NOT, AND, OR, NAND, NOR logic gate their graphic symbols & truth tables.**

*Ans :* **(Imp.)**

Logic gates from one of the major components of logic circuits. Using these gates certain define logic can be deployed in circuits. Each of them perform in a different manner. Functionality of these gates can be expressed by means of special tables referred as truth tables.

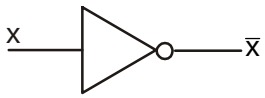
Types of logic gates

The different types of logic gates are :

1. NOT gate
2. AND gate
3. OR gate
4. NAND gate
5. NOR gate
6. X - OR gate
7. X - NOR gate

**1. NOT gate**

A NOT gate performs the inverse operation, i.e., when input is 'O' it gives 'I' as output and vice versa. The symbol of NOT gat is as shown in fig.

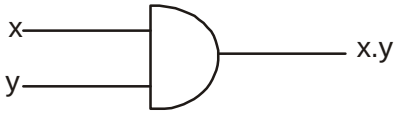



The truth table of NOT gate is shown in table (1).

| X | $\bar{X}$ |
|---|---|
| 0 | 1 |
| 1 | 0 |

## 2. AND gate

An AND gate performs the multiplication operation. It has two (or) more number of inputs and a single output. The symbol of AND gate is as shown in figure(3).



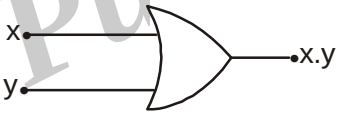

The truth table of AND gate is shown in table

| x | y | z = x.y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The AND gate output is '1' if all the inputs are '1' else, output is '0'

## 3. OR gate

An OR gate performs the logical addition operation it has two (or) more inputs and one output. The graphic symbol of OR gate is as shown in figure.

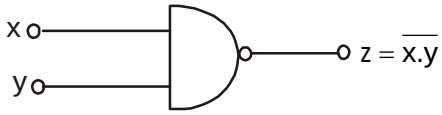



The truth of OR gate is shown in table

| x | y | z = x + y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## 4. NAND gate

A NAND gate is obtained by the combination of NOT and AND gate i.e., AND gate followed by NOT gate. It produces inverted output of AND gate. The graphic symbol of NAND gate is as shown in fig.



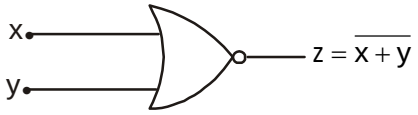

The truth table of NAND gate is shown in table.

| x | y | $z = \overline{x.y}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The output of NAND gate is '0' when both the inputs are '1'. When any one of the input is '0', output is '1'.

### 5. NOR gate

A NOR gate produces complemented output of OR gate. It is obtained by combining OR and NOT gate i.e., OR gate followed by NOT gate. The graphic symbol of NOT gate is as shown in fig.




The truth table of NOR gate is shown in table.

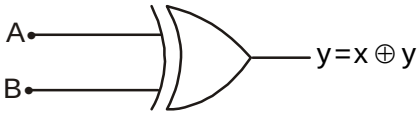
| x | y | $z = \overline{x + y}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

The NOR gate output is '1' when all the inputs are 0.

When any one the input is '1' its output is '0'.

### 6. X - OR gate

The X - OR gate graphic symbol is as shown in fig.



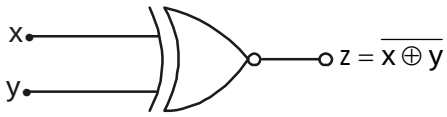

The truth table of X - OR gate is shown in table

| x | y | $z = x \oplus y$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The X-OR gate output is '1' only if one of the input is '1' otherwise, its output is '0' i.e., for odd number of '1' s, output is '1'.

### 7. X - NOR gate

The X-NOR gate is a combination of NOT and X-OR gate i.e., (x - OR gate followed by a NOT gate). The graphic symbol of X-NOR gate is as shown in figure.




The truth table of X-NOR gate is shown in table.

| x | y | $z = \overline{x \oplus y}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The output X-NOR gate is '1' when both the inputs are same i.e., '0' (or) '1' when both the inputs are different the output is '0'.

## 4.11 Logic Gates by Discrete Components

**Q15. Explain realization of logic gates by discrete components.**

*Ans :* **(Imp.)**

An OR gate performs the logical addition operation of two (or) more inputs.

**OR gate using Diodes**

An OR gate can be implemented using diodes. For instance, figure below represents a 2-input OR gate where output is high if any of the input is high.

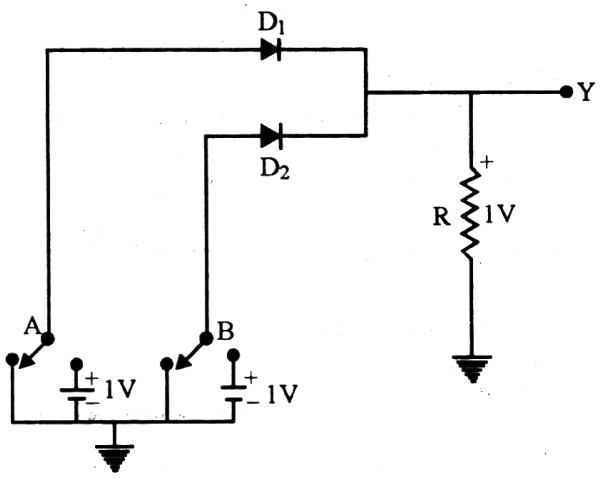



**Fig.: A two input OR gate using diodes**

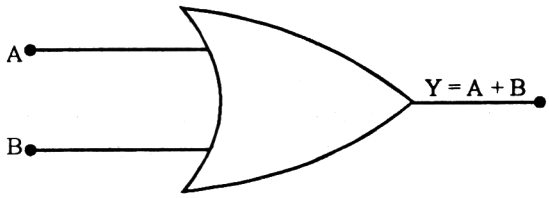



**Fig.: Circuit symbol of an OR logic**

Table below illustrates the inputs, condition of diodes and their respective out.

| Inputs | | Outputs |
|---|---|---|
| **A** | **B** | **y** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## AND gate

An AND gate performs the multiplication operation of two (or) more inputs.

## AND gate using Diodes

An AND gate can be implemented using diodes for instance, figure below represents a 2-input AND gate where output is high only if both the inputs are high.

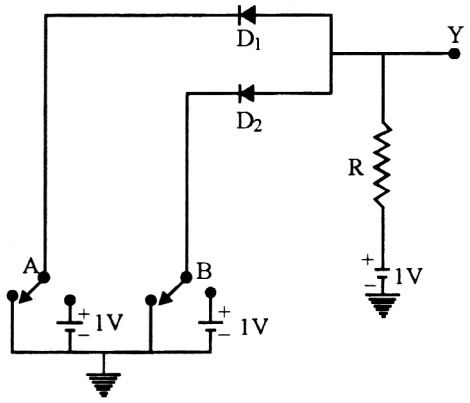



**Fig.: Diode AND Gate**

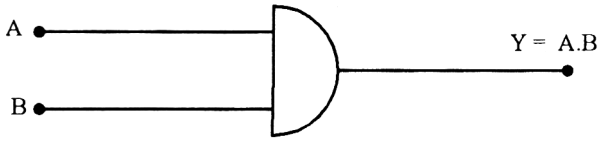



**Fig.: Circuit Symbol For AND Gate**

The inputs and their respective outputs are illustrated in table as,

| Inputs | | Outputs |
|---|---|---|
| A | B | y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**The NOT gate OR inverter circuit**

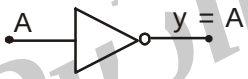
Another example of the basic digital circuits is the NOT gate. A NOT circuit has one input and one output. It inverts the polarity of a pulse applied to it. Thus a NOT circuit serves to negate the input function. If A is the input, then 'Output y Equal NOT A'. Thus is output is NOT the same as its input. The Boolean.

Expression for inverter is written as,

$$y = \overline{A}$$

where, the bar over a represents NOT. Hence if the letter A represent DOWN level (0), $\overline{A}$ represents UP(1) and if A = 1, $\overline{A}$ = 0

The truth table for NOT operation is given below




Truth table

NOT operation

| Input A | Output y |
|---|---|
| 0 | 1 |
| 1 | 0 |

A NOT circuit. In the grouped emitter configuration, the output is taken from the collector. When no signal is applied at the input i.e., A = OV, the transistor will be cut OFF and the output y will go to $V_{cc}$. Thus when input is law.

## 4.12 NAND, NOR AS UNIVERSAL GATES

**Q16. Show that NAND gate is universal building block.**

*Ans :* **(Imp.)**

**NAND gate as Universal Building Block**

The logic gates NAND and NOR are known as universal logic gates. In general, any boolean expression can be implemented using AND, OR and NOT gates. While, these basic gates can be implemented using NAND (or) NOR gate alone. This specifies that NAND (or) NOT gate alone can be used to implement any boolean expression. Hence NAND and NOR gates are termed as universal logic gates.

### Realization of logic gates using NAND gate

The truth table of NAND gate is shown

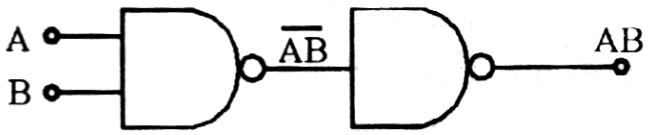
| Inputs | | Outputs |
|---|---|---|
| A | B | y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

### (i) And Implementation

The truth table of AND gate is show in table

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

From the table (1) and (2), the implementation of AND logic using NAND gate can be obtained as shown in figure.

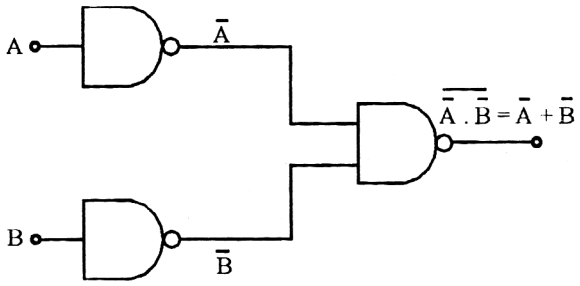



### (ii) OR Implemention

The truth table of OR gate is show in table

| Input | | Output |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

From the tables (1) and (3), the implementation of OR logic using NAND gate can be obtained as shown in figure.

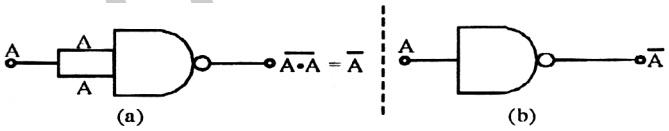



### (iii) NOT implementation

The truth table of AND gate is show in table

| Input A | Output Y |
|---|---|
| 0 | 1 |
| 1 | 0 |

From the table (1) and (4), the implementation of NOT logic using NAND gate can be obtained as shown in figure.




## NOR gate as universal gate

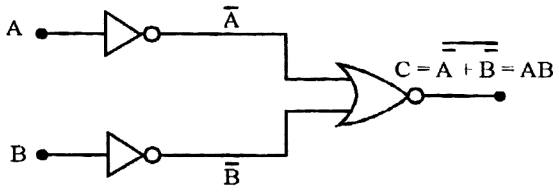
**Q17. Shown that the NOR as universal gate ?**

*Ans :*

The boolean function can also be implemented by using NOR gates. The NOR gates can be used for the implementation of OR, AND and complement operation.

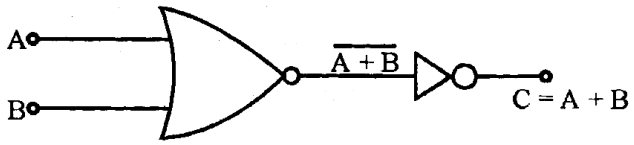
**AND Implementation**

The AND operation implementation requires a NOR gate which has inverters in each input. Figure (1), represent the implementation of AND gate using NOR gate.



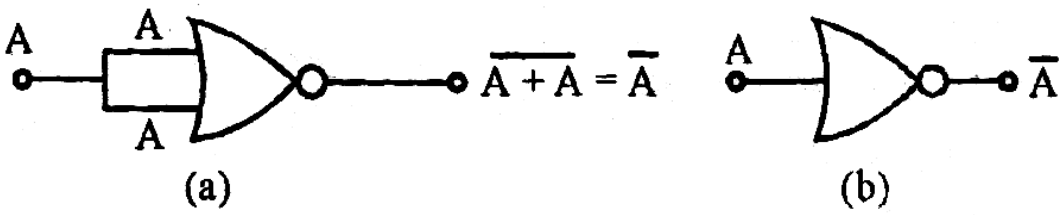
**OR Implementation**

The OR operation can be implemented by using two NOR gates as shown in figure.




**NOT (complement) Implementation**

The not operation can be implemented by using one input NOR gate as shown in figure.




## 4.13 EXCLUSIVE - OR GATE [EX - OR]

**Q18. What is boolean Equation for output of an X - OR gate ? What is symbol for it ?**

*Ans :*

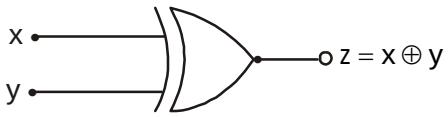
The boolean Equation for output of an X - OR gate is $Z = x \oplus y$

The truth table of X - OR gate is shown in table

| x | y | $z = x \oplus y$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The X - OR gate output is high only if one of the input is 1 otherwise, its output is low i.e., 0.

For odd number of is, output is '1'



## 4.14 DEMORGAN'S LAWS VERIFICATION

**Q19. State & prove De- morgan's theorems - Draw the relevant logic diagrams?**

*Ans :*

**Statement**

For any two variable 'A' and 'B' in boolean algebra, the complement of sum of logic variables is equal to the product of their individual complements.

i.e., $\overline{A+B} = \bar{A}.\bar{B}$

**Proof**

De-Morgan's theorem-1 can be proved by using truth tables as,

LHS

| A | B | $A+B$ | $\overline{A+B}$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 |

RHS

| A | B | $\bar{A}$ | $\bar{B}$ | $\bar{A}.\bar{B}$ |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |

**Fig. : a**

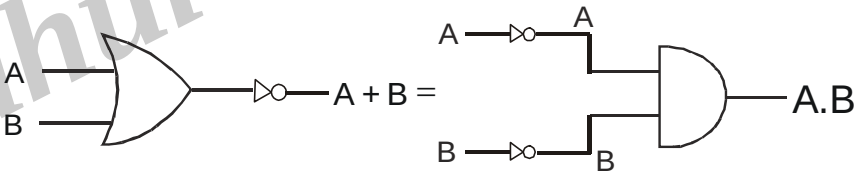



**Fig. : (a)**

$\therefore \quad \overline{A+B} = \bar{A}.\bar{B}$

Figure (1) represents the relevant logic diagram of De morgan's theorem-1

**De morgan's theorem -2**

**Statement**

For any two variable 'A' and 'B' in Boolean algebra, the complement of the product of logic variables is Equal to the sum of their individual complements.

i.e., $\overline{A.B} = \bar{A} + \bar{B}$

**Proof**

De Morgan's theorem-2 can be proved by using truth tables as,

LHS

| A | B | AB | $\overline{A.B}$ |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

RHS

| A | B | $\bar{A}$ | $\bar{B}$ | $\bar{A}+\bar{B}$ |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |

**Fig. : ( b)**

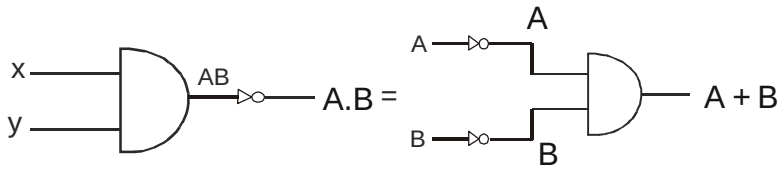



**Fig. : (b)**

$\therefore \overline{A.B} = \bar{A} + \bar{B}$

# Short Question and Answers

**1. What is binary number system? Explain with suitable example.**

*Ans :*

A system that represents a number with a combination of only two digits i.e., '0' and '1' is known as binary number system. In this system, each binary digit is referred as 'bit'. The base/ radix of a binary number is '2'.

For example, a binary number is represented as $(1101001)_2$ and the weight / value of each bit is expressed as a power of '2'. The left most bit process largest weight and is termed as most significant bit(MSB). Similarly, the right most bit possess smallest (or) least weight and is known as least significant bit(LSB). Any binary number can be converted into decimal number by adding all the bits multiplied by their weights. Table (2) shows the binary bits their weights expressed in powers of 2.

| Position | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
|---|---|---|---|---|---|---|---|
| Digit | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| Weight | $1\times2^6$ | $1\times2^5$ | $0\times2^4$ | $1\times2^6$ | $0\times2^2$ | $0\times2^1$ | $1\times2^0$ |
| | | MSB | | | | | LSB |

i.e., $1101001 = (1 \times 2^6) + (1 \times 2^5) + (0 \times 2^4) + (1 \times 2^3) + (1 \times 2^2) + k\,(0 \times 2^1) + (1 \times 2^0)$

$= 64 + 32 + 0 + 8 + 0 + 0 + 1 = 105$

$\therefore \quad (1101001)_2 = (105)_{10}$

**2. Explain 1's & 2's complement of binary addition.**

*Ans :*

The usual practice in computers is to change the substraction to an addition process. Thus the circuity is simplified because only adder circuits are needed for both addition and substraction.

In digital work, two types of complements of a binary number are used.

**(a) 1's complement**

The 1's complement of a binary number is the number which is obtained by changing its each 0 into a 1 and each 1 into a 0. For example, 1's complement of the binary number 1011 is 0100, and of 10011 is 01100.

**(b) 2's complement**

The 2's complement of a binary number is the number which is obtained by adding 1 to its 1's complement.

Thus,

2's complement = 1's complement + 1

Thus the 2's complement of binary number 1011 is 0100 + 1 = 0101.

The following table gives is and 2's complements of some binary numbers.

| Binary number | 1's complement | 2's complement |
|---|---|---|
| 100 | 011 | 100 |
| 101 | 010 | 011 |
| 1010 | 0101 | 0110 |
| 1011 | 0100 | 0101 |
| 1110 | 0001 | 0010 |
| 10100 | 01011 | 01100 |

**3. Explain converting hexadecimal to decimal.**

*Ans :*

To convert from hexadecimal to decimal we put the value of each digit from Table of sec. 1019, then multiply each digit by its weight and add the resulting products.

To explain, consider an example to convert $3C8_{16}$ to its decimal equivalent. Then

$$3C8_{16} = 3 \times 16^2 + 12 \times 16^1 + 8 \times 16^0$$

$$= 768 + 192 + 8 = 968_{10}$$

Here we have replaced C by decimal 12 from table of section.

Consider, another example to convert $E5F_8$ to decimal.

$$E5F8_{16} = 14 \times 16^3 + 5 \times 16^2 + 15 \times 16^1 + 8 \times 16^\circ$$

$$= 57344 + 1280 + 240 + 8$$

$$= 58{,}872_{10}$$

**4. Explain converting decimal to hexadecimal.**

*Ans :*

For it a hex-dabble method is used in which, a decimal number is successively divided by 16. The remainders are converted to hex notations and read in the reverse order i.e., from bottom to top.

**For example:** Convert $72905_{10}$ to hexadecimal.

Then

| Successive Division | Remainder | Hexnotations |
|---|---|---|
| 16 \| 72905 | 9 | 9 ↑ |
| 16 \| 4556 | 12 | C |
| 16 \| 284 | 12 | C |
| 16 \| 17 | 01 | 1 |
| 16 \| 1 | 01 | 1 |
| 0 | | |

Reading the remainders from bottom to top, the result is $11CC9_{16}$. Thus

$$72905_{10} = 11CC9_{16}$$

Consider another example to convert $423_{10}$ to hexadecimal. 16 1423

| | | |
|---|---|---|
| 16 \| 423 | 7 | 7 ↑ |
| 16 \| 26 | 10 | A |
| 16 \| 1 | 1 | 1 |
| 0 | | |

Thus, $423_{10} = 1A7_{16}$

**5. What are logic gates?**

*Ans :*

Logic gates from one of the major components of logic circuits. Using these gates certain define logic can be deployed in circuits. Each of them perform in a different manner. Functionality of these gates can be expressed by means of special tables referred as truth tables.

Types of logic gates

The different types of logic gates are :

1. NOT gate
2. AND gate
3. OR gate
4. NAND gate
5. NOR gate
6. X - OR gate
7. X - NOR gate

**6. Explain the NOT gate OR inverter circuit.**

*Ans :*

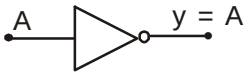
Another example of the basic digital circuits is the NOT gate. A NOT circuit has one input and one output. It inverts the polarity of a pulse applied to it. Thus a NOT circuit serves to negate the input function. If A is the input, then 'Output y Equal NOT A'. Thus is output is NOT the same as its input. The Boolean.

Expression for inverter is written as,

$$y = \overline{A}$$

where, the bar over a represents NOT. Hence if the letter A represent DOWN level (0), $\overline{A}$ represents UP(1) and if A = 1, $\overline{A} = 0$

The truth table for NOT operation is given below




Truth table

NOT operation

| Input A | Output y |
|---|---|
| 0 | 1 |
| 1 | 0 |

A NOT circuit. In the grouped emitter configuration, the output is taken from the collector. When no signal is applied at the input i.e., A = OV, the transistor will be cut OFF and the output y will go to $V_{cc}$. Thus when input is law.

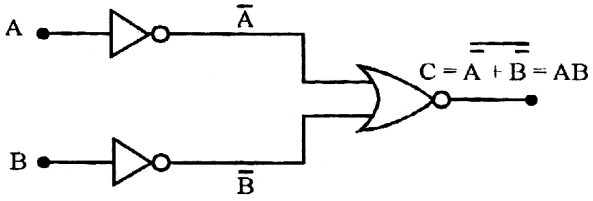
**7. Shown that the NOR as universal gate.**

*Ans :*

The boolean function can also be implemented by using NOR gates. The NOR gates can be used for the implementation of OR, AND and complement operation.

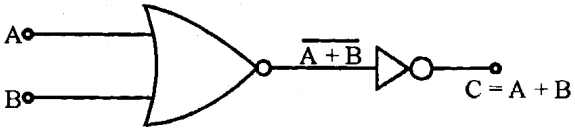
**AND Implementation**

The AND operation implementation requires a NOR gate which has inverters in each input. Figure (1), represent the implementation of AND gate using NOR gate.



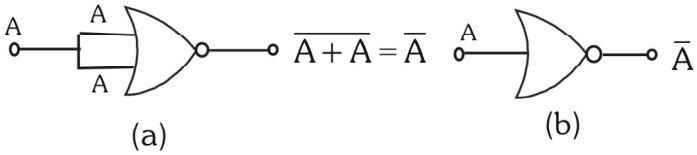

**OR Implementation**

The OR operation can be implemented by using two NOR gates as shown in figure.




**NOT (complement) Implementation**

The not operation can be implemented by using one input NOR gate as shown in figure.



# Choose the Correct Answers

1. 1's complement of $(1101)_2$ is [ b ]

   (a) $(0101)_2$ (b) $(0010)_2$

   (c) $(1100)_2$ (d) $(0011)_2$

2. Which among the following is a universal gate ? [ d ]

   (a) NAND (b) NDR

   (c) XOR (d) a and b

3. The decimal equivalent of binary number (1101) is [ a ]

   (a) 13 (b) 12

   (c) 11 (d) 10

4. In binary system 10 means [ c ]

   (a) 10 (b) 1

   (c) 2 (d) 0

5. The substraction two binary numbers $(0111)_2$ from $(101_21)$ gives [ b ]

   (a) 0101 (b) 0010

   (c) 1100 (d) 1010

6. Which of the following is an example of sequential gates [ d ]

   (a) OR & AND (b) NAND & NOR

   (c) XOR (d) Flip flops

7. AND gate provides high output when the inputs are respectively [ d ]

   (a) 0,0 (b) 0,2

   (c) (0,0) (d) (1,1)

8. $\overline{A.B}$ = according to DeMorgan's theorem 2. [ b ]

   (a) A + B (b) $\bar{A} + \bar{B}$

   (c) $\overline{A + B}$ (d) $\bar{A} + \bar{B}$

# Fill in the blanks

1. The digital signals are binary coded and are designed by _____
2. _____ can be obtained by adding '1' to its '1' is complement.
3. The binary number $(110111)_2$ when converted to decimal gives the value _____
4. Circuits which are used to process digital signals are called _____
5. The output of OR gate is LOW only when both the input are _____
6. Not gate is also known as _____
7. The output of exclusive OR gate is given by _____
8. A logic circuit that adds two bits producing a sum and a carry to be used in the next higher position is called _____
9. _____ is an example of XOR gate.
10. AND gate can be produced by connecting two NAND gates in _____



## ANSWERS

1. 0 and 1
2. 2's complement
3. $(55)_{10}$
4. Logic gates
5. Low
6. Inverter
7. $x = A \oplus B = A\bar{B} + \bar{A}B$
8. Half - Adder
9. Parity checker
10. Series

# FACULTY OF SCIENCE

## B.Sc. VI Semester (CBCS) Examination

## Subject : Physics

## Paper-VI : Electronics

## MODEL PAPER - I

Time : 3 Hours] [Max. Marks : 80

**Part - A (8 × 4 = 32 Marks)**

**Note : Answer any Eight questions**

**ANSWERS**

1. Explain the Introduction of Energy band? **(Unit-I, SQA-1)**
2. Distinguish between avalanche and Zenerbreakdown? **(Unit-I, SQA-5)**
3. What is Zener diode? **(Unit-I, SQA-3)**
4. What is meant by transistor biasing, (or) Different types of transistors? **(Unit-II, SQA-1)**
5. Derive the relation between $\alpha$ & $\beta$ ? **(Unit-II, SQA-5)**
6. How does transistor work as an amplifier? **(Unit-II, SQA-7)**
7. Compare BJT and MOSFET. **(Unit-III, SQA-2)**
8. Define photodiode? **(Unit-III, SQA-10)**
9. Which parameters greatly affect the oscillator frequency in the UJT relaxation oscillator? **(Unit-III, SQA-6)**
10. AB6.13 convert binary to hexadecimal. **(Unit-IV, Prob. 5)**
11. What is binary number system? Explain with suitable example.. **(Unit-IV, SQA-1)**
12. Explain converting decimal to hexadecimal. **(Unit-IV, SQA-4)**

**Part - B (4 × 12 = 48 Marks)**

**Note : Answer all the questions**

13. (a) Explain N-type & P-type Semi conductors? **(Unit-I, Q.No. 6)**

OR

(b) Explain and derive the Expression for Half wave Rectifier with neat sketches? **(Unit-I, Q.No. 11)**

14. (a) Explain about Bipolar junction transistor and its types ? **(Unit-II, Q.No. 1)**

OR

(b) Describe the construction and working of RC - coupled Amplifier. **(Unit-II, Q.No. 8)**

15. (a) Describe the construction and characteristics of photodiode and mention its uses. **(Unit-III, Q.No. 1)**

OR

(b) Define FET? Explain types of FET? **(Unit-III, Q.No. 6)**

16. (a) Explain converting of binary to decimal. **(Unit-IV, Q.No. 2)**

OR

(b) Show that NAND gate is universal building block. **(Unit-IV, Q.No. 16)**

# FACULTY OF SCIENCE

## B.Sc. VI Semester (CBCS) Examination

**Subject : Physics**

**Paper-VI : Electronics**

## MODEL PAPER - II

Time : 3 Hours] [Max. Marks : 80

**Part - A (8 × 4 = 32 Marks)**

**Note : Answer any Eight questions**

**ANSWERS**

1. What is a PN Junction Diode ? **(Unit-I, SQA-2)**
2. Differentiate N-type and P-type semiconductor. **(Unit-I, SQA-6)**
3. Distinguish between conductors, semiconductors and insulators? **(Unit-I, SQA-9)**
4. What are transistor configurations? **(Unit-II, SQA-2)**
5. What is meant by current amplification factor? **(Unit-II, SQA-6)**
6. Explain how a transistor acts as an oscillator. **(Unit-II, SQA-9)**
7. What are the important features of FET? **(Unit-III, SQA-3)**
8. State the application of the UJT? **(Unit-III, SQA-7)**
9. Explain classification of FET? **(Unit-III, SQA-8)**
10. $(5B8E)_{16}$ into decimal system **(Unit-IV, Prob. 8)**
11. Explain converting hexadecimal to decimal. **(Unit-IV, SQA-3)**
12. Explain the NOT gate OR inverter circuit. **(Unit-IV, SQA-6)**

**Part - B (4 × 12 = 48 Marks)**

**Note : Answer all the questions**

13. (a) Explain position of fermi level in Intrinsic & Extrinsic semiconductor? **(Unit-I, Q.No. 7)**

OR

(b) Explain & Derive the Expressions for Full wave Rectifier ? **(Unit-I, Q.No. 12)**

14. (a) Explain the operation of P-N-P transistor? Explain three operation of NPN transistor. **(Unit-II, Q.No. 2 and 3)**

OR

(b) Explain the barkhausen criterion for oscillations. **(Unit-II, Q.No. 9)**

15. (a) Explain working and V-I characteristics of schokley diode? **(Unit-III, Q.No. 2)**

OR

(b) What is MOSFET? Explain working and types of MOSFET? **(Unit-III, Q.No. 7)**

16. (a) Explain converting form binary to Hexadecimal. **(Unit-IV, Q.No. 10)**

OR

(b) What are logic gates? Explain about NOT, AND, OR, NAND, NOR logic gate their graphic symbols & truth tables. **(Unit-IV, Q.No. 14)**

# FACULTY OF SCIENCE

## B.Sc. VI Semester (CBCS) Examination

### Subject : Physics

### Paper-VI : Electronics

## MODEL PAPER - III

Time : 3 Hours] [Max. Marks : 80

**Part - A (8 × 4 = 32 Marks)**

**Note : Answer any Eight questions**

| | | ANSWERS |
|---|---|---|
| 1. | Distinguish between intrinsic and extrinsic semiconductors. | **(Unit-I, SQA-4)** |
| 2. | Difference between Half wave and Full wave rectifier? | **(Unit-I, SQA-7)** |
| 3. | Difference between pn junction diode and zener diode? | **(Unit-I, SQA-8)** |
| 4. | Define current Amplification factor. | **(Unit-II, SQA-3)** |
| 5. | What is meant by base current amplification factor? | **(Unit-II, SQA-4)** |
| 6. | Give the general theory of feed back. | **(Unit-II, SQA-8)** |
| 7. | Define FET? | **(Unit-III, SQA-1)** |
| 8. | Define, Silicon Controlled Rectifier (SCR)? | **(Unit-III, SQA-4)** |
| 9. | Which parameters greatly affect the oscillator frequency in the UJT relaxation oscillator? | **(Unit-III, SQA-6)** |
| 10. | Explain 1's & 2's complement of binary addition. | **(Unit-IV, SQA-2)** |
| 11. | What are logic gates? | **(Unit-IV, SQA-5)** |
| 12. | $(5B6E)_{16}$ convert into decimal form. | **(Unit-IV, Prob. 9)** |

**Part - B (4 × 12 = 48 Marks)**

**Note : Answer all the questions**

13. (a) Discuss on the basis of forbidden band about insulators, conductors & semi-conductors? **(Unit-I, Q.No. 3)**

OR

(b) What is junction diode ? Explain the formation of Depletion region at the junction. Explain the variation of depletion region in forward and reverse-biased condition. **(Unit-I, Q.No. 9)**

14. (a) What are the current components in transistors ? **(Unit-II, Q.No. 4)**

OR

(b) Describe the working of phase shift oscillator. **(Unit-II, Q.No. 11)**

15. (a) What is opto coupler, explain working and applications. **(Unit-III, Q.No. 4)**

OR

(b) Explain the construction and working of UJT. Explain its characteristics. **(Unit-III, Q.No. 9)**

16. (a) Explain converting of decimal to binary conversion. **(Unit-IV, Q.No. 4)**

OR

(b) Explain realization of logic gates by discrete components. **(Unit-IV, Q.No. 15)**